about the y-axis with an angular velocity of ω_p. If the construction of the gyroscope is perfectly symmetrical, there should be no rocking of the diaphragm about the x-axis and hence no net change in capacitance (i.e. zero signal) at the secondary sense due to the primary motion. In the presence of an applied rate of turn (Ω) about the z-axis, a secondary motion about the y-axis will be initiated owing to the Coriolis force. In a perfectly symmetrical structure, this excitation will coincide with the resonant frequency of the secondary motion and the diaphragm will rock about the x-axis with an angular velocity of ω_x. The resulting change in capacitance at the secondary sense will give a measure of w_x and hence the rate of turn about the z-axis.

Results: The following results were obtained, with a DC bias of 5V, a pressure of 1.7mB and a closed-loop primary motion angular velocity amplitude of 80rad/s at a resonant frequency and Q-factor of nominally 16kHz and 500, respectively. From a measurement of the modes of vibration of the primary and secondary motions, the resonant frequency of the secondary motion was found to be greater than that of the primary by 600Hz. This difference is due to mechanical asymmetries resulting from the fabrication of the gyro.

When the gyro is rotated with its primary motion at resonance, the output voltage signal of the preamplifier connected to the secondary sense was found to be determined not only by the rate of turn but also by mechanical and electrical coupling. These components, as will be shown below, can be modelled in terms of current sources, shown in Fig. 2, which all have a frequency equal to that of the primary motion.

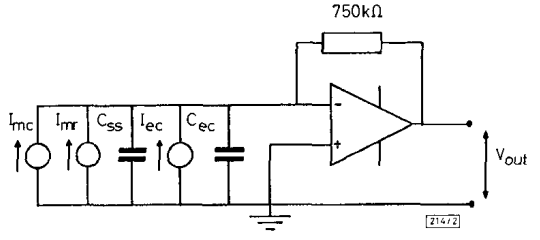

Fig. 2 *Secondary sense equivalent circuit*

Electrical interference is due to capacitive coupling between the primary drive and secondary sense electrodes. This has been reduced considerably by employing a guard ring, shown in Fig. 1*a*, and a bottom electrode on the opposite side of the Pyrex substrate to the electrodes, both of which are earthed. From a frequency analysis at atmospheric pressure (i.e. negligible diaphragm motion), the residual electrical coupling was found to be equivalent to a current source I_{ec} (amplitude 5×10^{-10} A and phase 90° relative to the primary drive voltage) in parallel with a capacitance C_{ec} (3.5×10^{-15} F).

The AC produced at the secondary sense due to the small mechanical motion of the diaphragm, is given by

$$I_m = V\frac{dC_{ss}}{dt} + C_{ss}\frac{dV}{dt} \qquad (1)$$

where C_{ss} is the capacitance and V is the voltage on the secondary sense. I_m is therefore equivalent to a current source in parallel with a capacitance C_{ss} (3pF). The current source is composed of I_{mc} (amplitude 4×10^{-8} A and phase 180° relative to the primary drive voltage), which is due to direct mechanical coupling of the primary motion arising from gyro asymmetry and $I_{mr} = k\,\omega_p\,\Omega$ resulting from the applied rate of turn, where k is a constant of proportionality determined by the voltage V, capacitance C_{ss} and the Coriolis coupling of the primary and secondary motions which is a function of mechanical asymmetry. For a 600Hz difference between the primary and secondary resonant frequencies, the phase of I_{mr} relative to the primary drive voltage was expected to be 90°. Thus by employing phase-sensitive detection techniques, I_{mr} was resolved from the much larger value of I_{mc} to detect rates of turn down to ±300°/s. A linear response with rate of turn was obtained, which, when extrapolated, passed through the origin. For a rate of turn of 1000°/s, the amplitude of I_{mr} was found to be 10^{-10} A, which agreed well with theoretical predictions.

Discussion: A silicon microdynamic gyroscope employing a loaded membrane has been constructed and tested. The results to date indicate that the performance is mainly limited by mechanical asymmetries which result in a loss of response and the production of a mechanical bias signal far in excess of that due to rate of turn. This bias signal can arise from a number of sources, all of which are related to the asymmetry of the structure and include: (i) misalignment of the electrode pattern relative to the axis x, y and z, (ii) poor mass distribution about the centre of the diaphragm; (iii) different diaphragm stiffnesses about the x- and y axes. A detailed study of the precise causes of the asymmetry; in particular the wet etching techniques used to fabricate the diaphragm and inertial mass is being carried out. The most likely cause is (ii) owing to the presence of secondary etch planes at the pyramid corners, not shown in Fig. 1*a*, which are not equally developed at all four corners. The next most important factor limiting performance is electrical coupling from the primary drive to the secondary sense. Initial tests have shown that this is determined by coupling through the Pyrex substrate and significant improvements are possible by reducing its thickness. For a mechanically symmetrical structure of the same size and operating conditions as described above, where the electrical noise due to the preamplifier is dominant, a noise equivalent rate of turn of 0.14°/s is predicted for a 100Hz bandwidth. This figure can be significantly reduced by increasing the diaphragm area/inertial mass, the primary motion amplitude, the DC bias voltage and the Q-factor.

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Digital IC device testing by transient signal analysis (TSA)

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Indexing terms: Integrated circuit testing, Electric current measurement, Pattern recognition, Neural nets

The Letter presents a new approach to testing digital circuits that uses the variations in the transient signals generated within digital circuits as a defect detection method. The I_{DD} transients on the supply rails and voltage transients at selected test points are sampled over a test interval. Simulation experiments show that variations in the transient waveforms between defective and nondefective circuits exist and that these variations are sensitive to many types of defects even when they appear on off-sensitised paths. These variations can be analysed using pattern recognition techniques, and neural processing is proposed as the means of identifying the transient waveforms of defective devices [1, 2].

Introduction: Parasitic resistances and capacitances are present in all digital ICs [3]. An ideal nondefective device can be characterised as having a well-defined set of parasitic components and therefore a predictable transient response. Alternatively, device defects add or remove parasitic elements from the AC network in the region of the defect. For example, a single open drain will remove a significant percentage of the normal parasitic capacitance present on the output node of a CMOS logic gate. Similarly, a bridging short-circuit between two or more logic gate output

lines adds new parasitic resistive and capacitive elements at each of the short-circuited nodes. However, in real devices the stochastic nature of the fabrication process also causes variations in the values of these parasitics. Consequently, the transient response of both defective and nondefective devices varies as a function of process parameters.

In this technique, a combination of global information taken from the I_{DD} transient response and local information from several test point voltage transients is capable of identifying defective devices in the presence of process variations. Since most components are directly coupled through the supply rails, changes in the transient response can be observed by monitoring the I_{DD} transients as an input stimulus propagates from primary inputs (PIs) to primary outputs (POs) [4, 5]. In many cases, the individual transistor switching transients representing the spatial variation in the parasitic networks can be resolved temporally in the resulting I_{DD} transient waveform. However, in large circuits, monitoring the I_{DD} transients alone may not provide sufficient defect resolution when a large number of transistors switch simultaneously. Defect resolution can be improved by taking advantage of the direct coupling that exists between transistors along the functional paths of the circuit and the capacitive coupling that exists between adjacent conductors. Therefore, by monitoring the voltage transient at a set of test points, regional defect detection is possible. By using both the I_{DD} and voltage transients and by propagating signals from PIs to POs, defect resolution is maximised since both temporal transient behaviour of the current and regional transient behaviour of the voltage are used in the decision process.

Experiments: A set of simulation experiments were conducted on defective and nondefective versions of the ISCAS85 c432 benchmark circuit. The c432 was automatically synthesised with OCTTOOLS (v5.1) using a subset of the ITD/AμE (Advanced Microelectronics Division) SCMOS standard-cell library (v2.2). The circuit model was created using the MAGIC (v6.43) extract procedure and the Hewlett-Packard CMOS26B parasitic extraction parameters obtained from MOSIS. SPICE (v3f4) simulations were run on the extracted circuits, with and without defects introduced, using the CMOS26B SPICE LEVEL=3 transistor models [6]. The test vector sequence used as input generated a high-going pulse on netlist PI line 17 through an MOSIS SCN-08 input pad. The other 35 PIs were held low. The transient voltage response of all seven POs as well as the I_{DD} transients were monitored. The raw waveforms collected were then postprocessed into signature waveforms (SWs) by subtracting the raw waveforms produced by test devices from a set of standard raw waveforms representing a nondefective standard device.

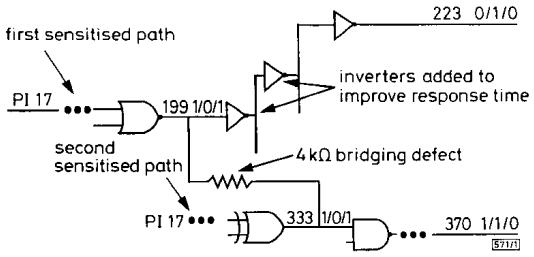

Fig. 1 *Portion of the ISCAS85 c432 benchmark schematic diagram II showing a bridging defect*

Results: Fig. 1 shows a portion of the c432 schematic diagram in which a 4kΩ bridging defect has been introduced between netlist lines 199 and 333 which appeared in the layout as adjacent metal 1 lines. The changes in the logic states at the bridged nodes are identical. Therefore, neither logic testing nor I_{DDQ} testing would detect this defect under the test vector sequence applied. This defect shorts the output lines of gates along two separate sensitised paths within the c432. Therefore, the logic state transitions indicated in the Figure occur at different times owing to the difference in the path delays from PI 17 to each of these lines. The corresponding SWs for voltage transients at all seven PO test points are shown in Fig. 2 and the I_{DD} transient SW is shown in Fig. 3. The ability of the technique to resolve the change in the transient response regionally is shown clearly in the SWs of POs 223, 329 and 370. The other POs were not affected. In this case, the I_{DD} SW also provides a strong indication that a defect exists.

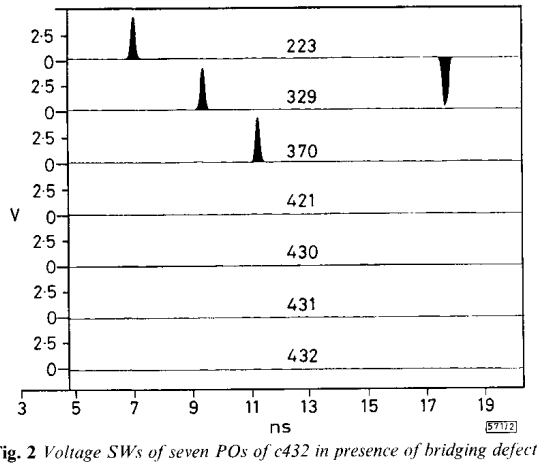

Fig. 2 *Voltage SWs of seven POs of c432 in presence of bridging defect*

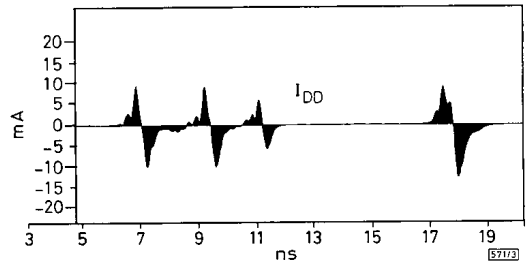

Fig. 3 *Current SW of supply rail of c432 in presence of bridging defect*

Other simulation experiments were conducted, to examine the SWs for defects that result in stuck-at, stuck-open and transistor stuck-on faults such that the fault behaviors were manifested on off-sensitised paths. Thus, the logic behaviour of the defective device was preserved under the test vector sequence. Experiments were also conducted with defects placed in logic gates that use redundancy to increase their current drive capability. In all cases the effect of the defect was observable in the SWs of one or more test points.

Another set of simulation experiments was conducted where process variation was modelled globally by changing transistor gate oxide thickness and the threshold voltage. In these cases, the shape of the transient SWs was preserved and only variations in magnitude were recorded. Moreover, the changes observed were consistent across all SWS. A third set of experiments were conducted in which both defects and process variation were introduced. In each case, the SWS of the defect and the process variation were superimposed and the regional variations introduced by the defects were still observable.

Conclusions: TSA offers several advantages over existing device testing techniques. The simulation experiments conducted on the c432 show that changes in the transient response of a defective circuit are observable at one or more test points and that the method is very sensitive to many types of defects. In this sense the method is based on a defect model rather than a fault model. Furthermore, the method is not invalidated in the presence of multiple defects, requires only a small number of test vectors and can be adapted easily to on-line testing.

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http://www.research.digital.com/wrl/projects/magic/magic.html
ftp://www.eecs.berkeley.edu/pub/Spice3Portion of the ISCAS85

500Mbit/s operation of a multifunctional binary optical switching fabric

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Indexing terms: Optical switches, Integrated optoelectronics, Heterojunction bipolar transistors, pin photodiodes, Vertical cavity surface emitting lasers

A cascadable binary optical routing switch with improved switching performance has been demonstrated by integrating vertical-cavity surface-emitting lasers with heterojunction bipolar transistors and *pin* photodiodes. The reconfigurable routing of optical signals, and their conversion between electrical and optical formats, have been achieved at high speed (400–500Mbit/s), and with an optical gain of 7.5dB.

A new switching fabric, consisting of vertical cavity surface emitting lasers (VCSELs), *pin* photodiodes (*pins*), and heterojunction bipolar transistors (HBTs) capable of operating at high speed (400–500Mbit/s) and high optical gain (7.5dB) has been demonstrated. VCSELs can be integrated with active electronic [1, 2] and photonic [3 – 5] devices to form optoelectronic switches that combine the functions of an optical transceiver [3] with those of a spatial routing switch [4]. A single switch integrating an HPT with a VCSEL has previously performed at a data rate of 200Mbit/s [3] but optical gain was not achieved, and routing was not incorporated into the design. We have improved the switching performance by separating the light detection and amplification functions, using a *pin* diode for photodetection, and an HBT for gain. This functional separation allows us to reconcile the conflicting requirements of high current gain, high optical coupling efficiency, and high speed, which constrained the design of the HPT and thus limited its performance.

Each node in the new switching fabric (Fig. 1) consists of a pair of *pin*/HBT/VCSEL switches, each containing a VCSEL connected to an HBT in an emitter-follower geometry, and a *pin* connected in parallel to the base-collector junction of the HBT. The two *pins* are closely spaced and form a single optical input port, whereas the VCSELs provide two spatially separated optical output ports. When an optical signal is incident upon the *pin* pair, two nearly identical photocurrents are generated, each of which is separately amplified by the HBT in the follower circuit. The amplified current in each circuit can be detected as an electrical current modulation at the collector terminal of the HBT or, depending on the control voltage V_c at the collector, the current can modulate the VCSEL to generate an optical output signal. Each VCSEL can also be modulated by an electrical input signal applied at the base terminal of the HBT, which is converted into an optical output signal via the VCSEL. Each switching node can thus act as an optical receiver (optical input, electrical output), a transmitter (electrical input, optical output) or an optical routing switch (one optical input, one or more optical outputs) with a fan-out of two. Fig. 1*b* shows the two closely spaced *pins* and their associated HBTs.

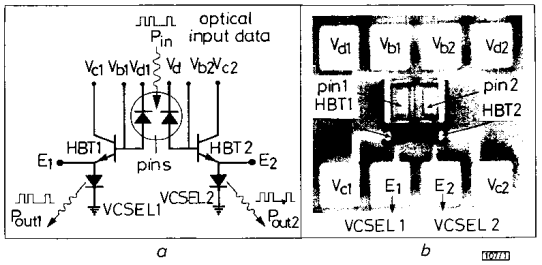

Fig. 1 *Circuit design and device layout of a reconfigurable binary switching node, consisting of two individually addressable pin/HBT/VCSEL switches*

a Circuit design
b Device layout

The HBT has an emitter-up configuration [4], and its lower base-collector junction layers are used to define the *pin*. The *pin* has an absorption length of ~0.6μm, and its absorption efficiency is ~45%. Assuming an uncoated surface with a Fresnel reflection loss of ~32%, the responsivity of the *pin* is estimated to be ~0.22 A/W at the operating wavelength λ = 850nm, compared to the experimentally determined value of ~0.2A/W. The measured –3dB bandwidth of the *pin* is 700MHz at a reverse bias of –5V.

The HBTs have a differential current gain of β = 70–100 at a collector current in the range of I_c = 5–15mA, corresponding to a current density of 5–15kA/cm². The –3dB modulation bandwidth of the HBT, measured with a coplanar probe setup, is 550MHz. The 16μm diameter VCSELs have high slope efficiencies ($\eta_s \simeq$ 5%), and produce a 1mW optical output at a current of 12mA and an operating voltage of 2.5V, but their threshold currents (I_{th} = 8.1mA) are relatively high.

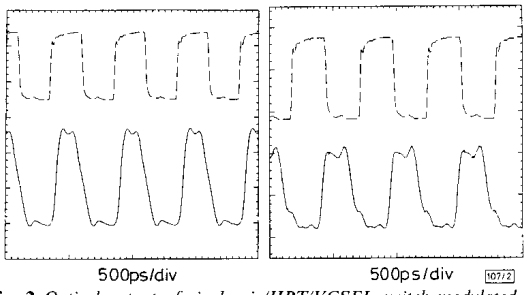

Fig. 2 *Optical output of single pin/HBT/VCSEL switch modulated at 400Mbit/s by electrical input signal and optical input signal*

a Electrical input signal
b Optical input signal
- - - input
——— output

Each *pin*/HBT/VCSEL switch is prebiased near the lasing threshold of the VCSEL with a DC base current of 220–280μA, yielding a DC emitter current of ~7.8mA. This reduces the switching time and eliminates the issue of the high threshold current of the VCSEL. Fig. 2*a* demonstrates the conversion of a large-amplitude electrical input signal to an optical output signal. The electrical input signal applied to the base of the HBT consisted of a train of pulses ~2.5ns wide and ~500mV in amplitude, representing 400 Mbit/s non-return-to-zero (NRZ) input data.

Fig. 2*b* demonstrates the optical-to-optical switching performance of the binary switch. The optical input is provided by a separate VCSEL, which is prebiased just below threshold and is