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Time- and Frequency-Domain Transient Signal Analysis for Defect Detection in CMOS Digital IC's

James F. Plusquellic, Donald M. Chiarulli, and Steven P. Levitan

***Abstract*— A novel approach to testing CMOS digital circuits is presented that is based on an analysis of voltage transients at multiple test points and $I_{\rm DD}$ switching transients on the supply rails. We present results from hardware experiments that show distinguishable characteristics in the transient waveforms of defective and nondefective devices. These variations are shown to exist in both the time domain and frequency domain for CMOS open-drain and bridging defects, located both on and off sensitized paths.**

***Index Terms*—CMOS defects, digital device testing, frequency domain, parametric, transient response.**

I. Introduction

Transient signal analysis (TSA) is a new parametric approach to testing digital integrated circuits [1], [2]. Defect detection is accomplished in TSA by analyzing the transient signals of a device measured simultaneously at multiple test points. The transient waveforms characterize the physical components of the device. Signal variations across devices result primarily from changes in the resistive, inductive, and capacitive components of the coupling network, as well as in the gain and threshold voltage characteristics of the transistors. Variations in the values of these circuit parameters may result from process tolerances, or they may result from defects.

The approach has two advantages over other logic and parametric testing methods. First, by analyzing small signal variations in the transient waveforms, TSA can detect the presence of defects at test points that are not on logic signal propagation paths from the defect site. This is possible because of the device coupling mechanisms, which include the resistive and capacitive coupling through the power supply and the wells, as well as parasitic capacitive and inductive coupling between conductors. The large signal variations of faults at defective nodes couple through adjacent conductors and produce small signal variations at test point nodes. The ability to detect defects, without requiring their faults to be propagated to observation points, improves the sensitivity of the device test and may reduce the test set generation size and complexity.

The second advantage of TSA is the use of multiple test point signals. By cross correlating the signals measured simultaneously at different topological locations on the device, it is possible to distinguish between signal variations caused by process tolerances and those caused by defects. This is true because process tolerance effects tend to be global, causing signal changes on all test points of the device. In contrast, signal variations caused by a defect tend to be regional and more pronounced on test points closest to the defect site.

In this paper, we present the results of four hardware experiments conducted on devices with bridging and open-drain defects. We demonstrate the regional and global signal variations that occur in the test devices by measuring the voltage transients at a set of test points located on probe pads on the surface of the die. We introduce signature waveforms (SW's) as a means of capturing signal variations in both the time- and frequency-domain representations of the test point waveforms. We show that the Fourier phase components of the frequency-domain SW's possess better discriminatory information than the magnitude- or time-domain SW's.

The remainder of this paper is organized as follows. In Section II, we present related research on device testing. Section II describes SW's. Section IV presents the results of hardware experiments conducted on devices with intentionally inserted bridging and open-drain defects. Section V presents our conclusions.

II. Background

Parametric device testing strategies [3]–[6] are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of quiescent supply current, or transient response. Many types of parametric tests have been proposed [7], but recent research interest has focused primarily on three types: $I_{\rm DDQ}$ [8], $I_{\rm DD}$ [9], and delay fault testing [10], [11].

$I_{\rm DDQ}$ is based on the measurement of an IC's supply current when all nodes have stabilized to a quiescent value [12]. $I_{\rm DDQ}$ has been shown to be an effective diagnostic technique for CMOS bridging defects, but is not applicable to all types of CMOS defects [13], [14]. Several dynamic supply current $I_{\rm DD}$-based approaches have since been proposed [9], [15]–[18]. In general, these $I_{\rm DD}$-based methods are not hampered by the slow test application rates and are not as sensitive to design styles as $I_{\rm DDQ}$. However, they do not provide a means of accounting for process tolerances and are therefore subject to aliasing problems.

Alternatively, delay fault testing takes advantage of the fact that many CMOS defects cause a change in the propagation delay of

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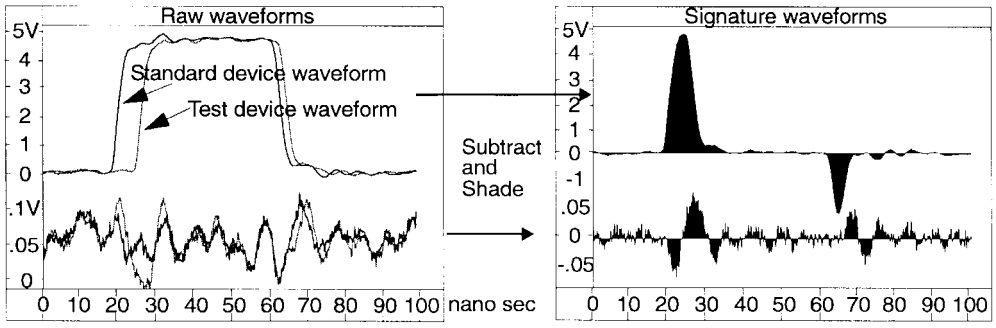

Fig. 1. Time-Domain SW creation procedure.

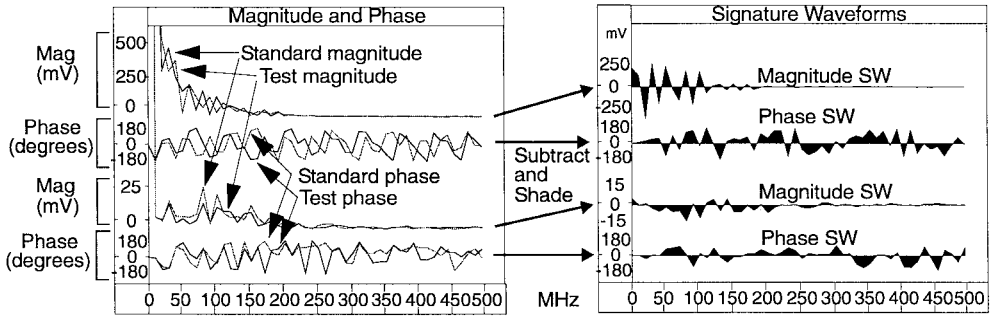

Fig. 2. Frequency-Domain SW creation procedure.

signals along sensitized paths [6]. Difficulties with delay fault testing include the complexity of test generation and path selection [19]–[21]. Franco and McCluskey [22] and others [23]–[25] have proposed extensions to delay fault testing that address some of these difficulties.

Recently, Ma *et al*. [26] and others [5], [6], [27], [28] evaluated a large number of test methodologies and determined that a combination of several test strategies may be necessary in order to find all defective devices. Our technique, TSA, with its advantages in defect detection and process insensitivity, is proposed as an addition to this test suite.

III. TSA Procedure

TSA is based on the analysis of transient signal variations. In order to capture the variations produced by defects in the test point signals, we create SW's using the procedure shown in Fig. 1. Shown in the upper portion of Fig. 1(a) are the transient waveforms generated by two devices at a test point located along a sensitized test path. Similarly, shown along the bottom are two transient waveforms produced by the same two devices at a nonsensitized test point. SW's are created from these pairs of transient waveforms by subtracting the test device waveform from the standard device waveform. The difference waveforms, shown in Fig. 1(b), are shaded along a zero baseline to add emphasis to the variations. The frequency-domain SW's are created by performing a discrete Fourier transform (DFT) on the raw time-domain waveforms, as shown in Fig. 2. Magnitude and phase SW's are created by subtracting the test device magnitude and phase values from the corresponding values of the standard device.

IV. Experimental Design

In this section we present the results of several hardware experiments, designed to demonstrate that it is possible to characterize IC's using time- and frequency-domain SW's. We designed three versions of the ISCAS85 c432 benchmark circuit [29], a version with

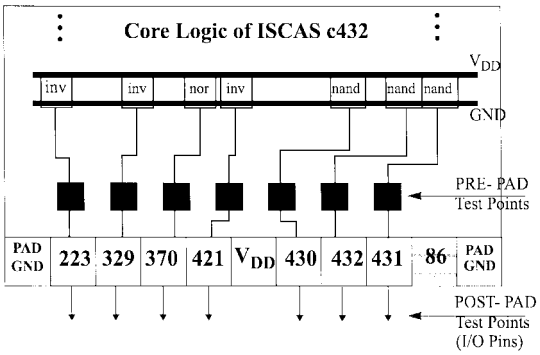

Fig. 3. Location of the test points on the c432.

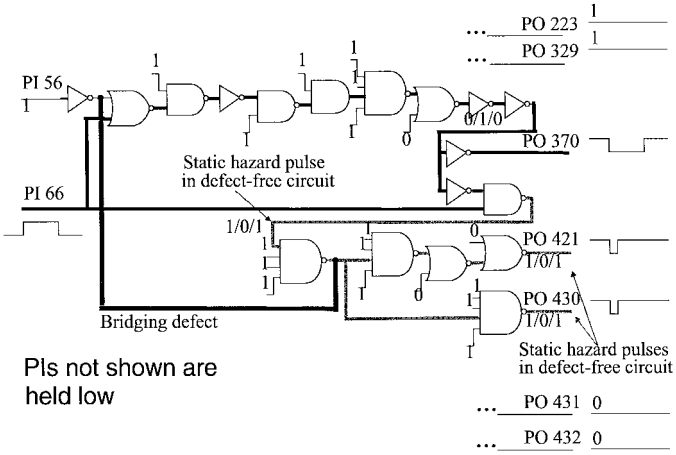

Fig. 4. Portions of the c432 schematic showing the short and the sensitized paths affected by the defect of Bridging Experiment 1.

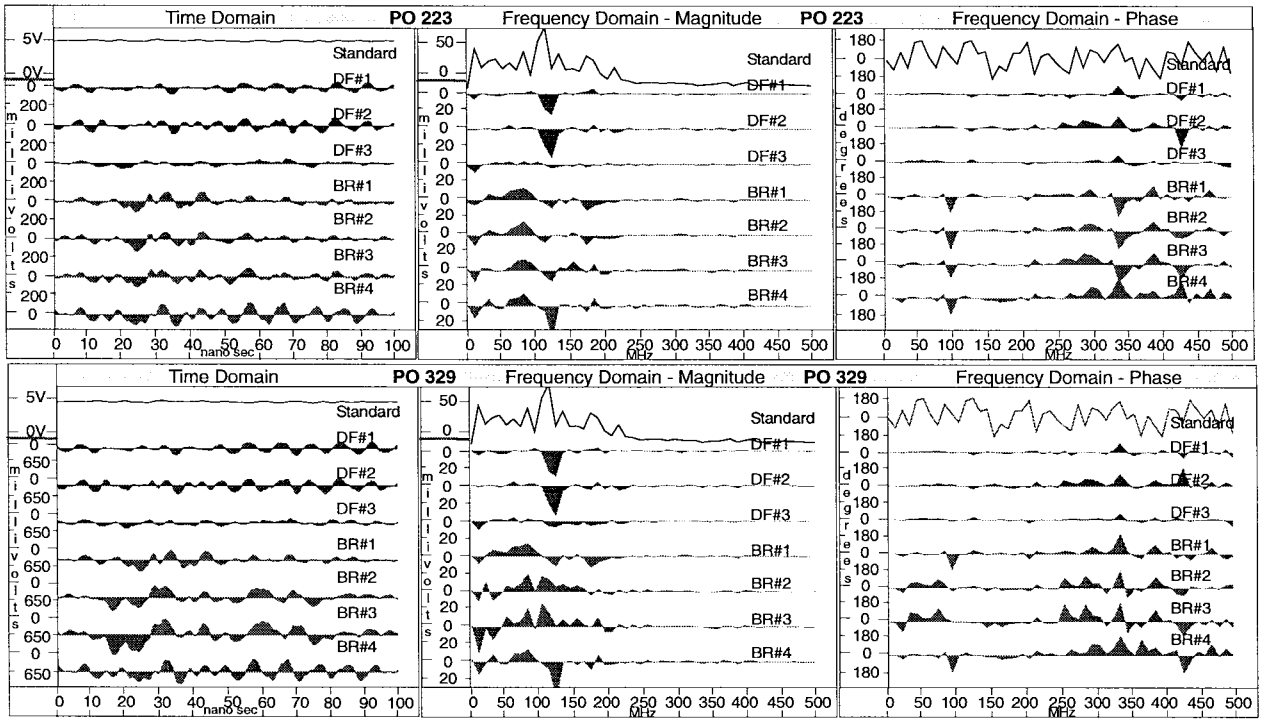

Fig. 5. Time- and frequency-domain SW's from PO's 223 and 329 of Bridging Experiment 1.

intentionally inserted bridging defects, a version with intentionally inserted open-drain defects, and a defect-free version. Four devices of each version were fabricated at MOSIS using ORBIT's 2.0-μm SCNA process. The defect-free devices were verified using both functional and stuck-at test sets.

The test points used in these experiments are labeled PRE-PAD and POST-PAD in Fig. 3. The reader is directed to [30] for a discussion of the POST-PAD results. The PRE-PAD test points are 22-μm square metal two pads placed on the output nodes of the gates driving the seven primary outputs of the c432. Since the test points are driven directly by the core logic, variations introduced through coupling mechanisms in the input–output (I/O) pads are reduced. Moreover, core logic test point measurements eliminate signal attenuation effects introduced by the I/O pad drivers. The measurements were taken at a probe station using a PicoProbe, model 12C, with a 100-FF and 1-MΩ load.

The TSA testing process involves applying a test vector sequence to the primary inputs (PI's) of an IC and sampling the waveforms generated at the test points. SW's extract only the variation that occurs between the test devices and the standard device. In each experiment four defect-free and four defective devices were tested. The same defect-free standard device was used in all experiments.

A. Bridging and Open-Drain Experiments

We report the results of the first bridging defect experiment and summarize the results of the other experiments. We analyze only the SW's of off-path test points in these experiments and demonstrate that the signal variations caused by defects are most easily measured as phase shifts in the frequency-domain SW's.

Fig. 4 shows a portion of the schematic diagram of the c432. The input stimulus for this experiment toggles PI 66 at 11 MHz. PI 56 is held high and the other PI's (not shown) are held low. The dotted line in the figure represents the bridging defect which was created in the layout by inserting a first-level to second-level metal contact between the output lines of the four-input NAND and the inverter. The only PO that changes logic state is 370. However, in the defect-free circuit, a static hazard causes a pulse to propagate to PO's 421 and 430 along the shaded paths shown in the figure. Note that the bridging defect is not on any sensitized path and no contention exists between the two bridged nodes in steady-state. However, since the output of the inverter driven by PI 56 is low, the bridge eliminates the pulse produced by the hazard in the defective devices. The large signal variation caused by the removal of the hazard couples into adjacent nodes. We demonstrate that it is possible to use the transient signals of nonsensitized test points 223, 329, 431, and 432 to identify the defective devices.

Each of the rows of plots in Fig. 5 shows a set of time-domain and frequency-domain SW's from a single test point identified in the header. The time-domain SW's are shown in the left plots while the magnitude and phase SW's are shown in the middle and right plots, respectively. The top waveform of each plot is the output trace from the standard defect-free IC used in the difference operation to create the SW's shown below it. The next three waveforms labeled DF#1–DF#3 are the SW's from each of the three remaining defect-free IC's. The next four SW's labeled BR#1–BR#4 are the SW's from the four *BRidging* defective IC's. Given that our objective is to identify defective devices using these waveforms, this format facilitates the comparison of the set of defect-free device SW's with the set of defective device SW's. The discussion that follows focuses on identifying distinguishable characteristics that occur in one set and not in the other.

As indicated in the schematic diagram of Fig. 4, PO's 223 and 329 remain steady-state high under the test sequence. The time and frequency-domain SW's for these test points are shown in Fig. 5. The most significant distinguishable characteristic that occurs between the sets of defect-free and defective SW's in the figure is illustrated in the phase plots on the right. In this case, phase shifts occur in the BR#1 and BR#4 SW's at 100 MHz and between 10 and 100 MHz in the BR#2 and BR#3 SW's. No significant variation occurs in the phase SW's of the defect-free devices below 250 MHz. The magnitude

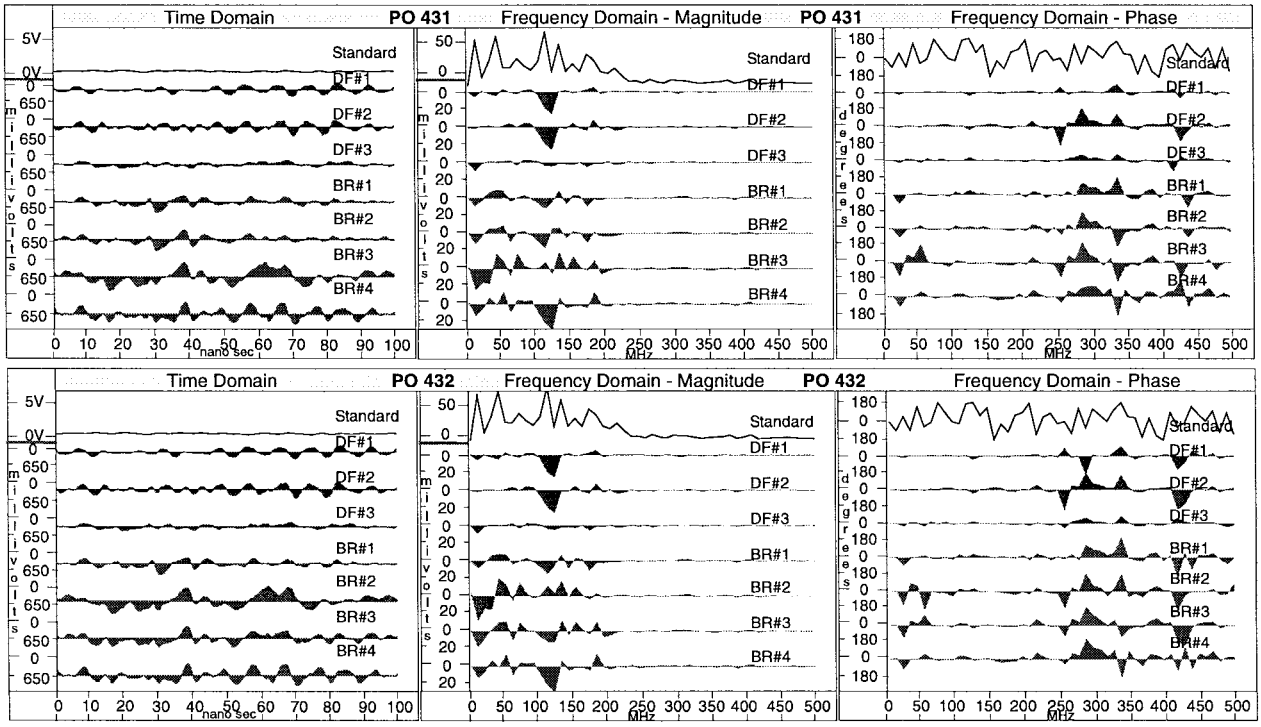

Fig. 6. Time- and frequency-domain SW's from PO 431 and 432 of Bridging Experiment #1.

SW's of the defective devices shown in the middle plots of these figures also show distinguishable variation in the region between 50 and 100 MHz. But the variation in the magnitude SW's of DF#1 and DF#2 at 125 MHz create an anomaly in the characterization of the defect-free devices. However, this anomaly can be attributed to process tolerances if the magnitude SW's of PO's 223 and 329 as well as PO's 431 and 432 (Fig. 6) are considered together. This is true because the variation is global in that it occurs at the same frequency and with the same relative magnitude in all four test point SW's. In summary, these results indicate that the defect delays and distorts specific frequency components of off-path signals. This phenomenon is difficult to see in the time-domain SW's of Fig. 5 because other frequency components combine to mask these variations.

The SW's for PO's 431 and 432 are shown in Fig. 6. PO's 431 and 432 remain at steady-state low under the test sequence. Again, we note specific phase shifts and distortions of magnitude in the phase and magnitude SW's of the defective devices while the time-domain SW's are nearly indistinguishable. More importantly, however, is the change in the frequency range of the phase shift in these outputs when compared with PO's 223 and 329. In this case, the phase components between 15 and 20 MHz are shifted by the defect. Unlike the variation caused by process tolerances observable in all magnitude SW's of devices DF#1 and DF#2, the difference in the phase behavior between these two sets of outputs suggests that this variation is due to a defect, since it is different depending on the logic state of the test point.

The second bridging experiment yielded similar results. The test sequence applied in the second experiment sensitized a path through both contact sites of a feedback bridging defect. The defect caused a significant delay in signal propagation along this path but did not cause a logic error. We reduced the frequency of the applied input stimulus to 1 MHz for this experiment. This allowed us to examine the transients generated as a single edge was propagated through the circuit under quiescent initial conditions, similar to the conditions of an impulse experiment. The magnitude and phase SW's of the nonsensitized test points closest to the defect site showed variation over the entire range of frequencies analyzed. Moreover, the slower input stimulus enhanced the variations that occurred between the defective and nondefective devices in the time domain.

The open-drain experiments provide further supporting evidence that defects cause regional signal variation that is best measured as phase shifts in the phase SW's. The open drains were introduced into four-input NAND gates by removing metal one between the p-transistor drain pairs. The test sequence for the first open-drain experiment caused logic signal transitions to occur on all but one of the test points. Variations caused by process tolerances were measurable as changes in propagation delay in both the defect-free and defective device time-domain SW's. However, the regional signal variation caused by the defect created distinct phase shifts at each of the test points that permitted the defective devices to be easily identified. Moreover, we observed a definite correlation between the change in propagation delay and the length of the sensitized path across the test points of each device in both open-drain experiments. The correlation of multiple test point signals can be used to identify the global variation caused by process tolerances and reduce the number of false positive and fault negative defect detections.

V. Conclusion

We presented a new parametric testing method for digital integrated circuits called TSA. We used hardware experiments to demonstrate that defect detection was possible using the signals at test points that were not on logic signal propagation paths from the defect site. We also showed that it was possible to distinguish between the variations caused by defects and those caused by process tolerances by correlating the SW's measured at distinct topological locations on the device.

We demonstrated that the phase SW's were more useful than the time and magnitude SW's in providing a means of discriminating between the defect-free and defective devices. We observed distinct phase shifts in the SW's of both bridging and open-drain defective

devices and no significant phase variation in the SW's of the defect-free devices. Moreover, the proximity of the test point to the defect site and its output state determined the frequency components that were affected. Both of these effects supported our expectation that the defect causes regional signal variations in the defective device.

The global effects of process tolerances were best illustrated in the magnitude SW's of nonsensitized test points and in the time-domain SW's of sensitized test points. We observed similar variations in the magnitude SW's of defect-free devices across all test points. We also noted a strong relationship between the magnitude of variation introduced by propagation delay and the length of the sensitized path in the time-domain SW's of defect-free devices. Both of these effects supported our expectation that process tolerance effects cause global signal variations that are proportional in all test point signals.

We are currently conducting a set of modeling experiments in order to characterize each of the coupling mechanisms, namely, the power supply, internodal, well, and substrate. We expect that the power supply is the predominant signal coupling mechanism and that measuring voltage transients directly on the supply rails would both increase the sensitivity of the test and reduce the number of test points required. The information obtained from the modeling experiments will help us determine the number and position of the test points and, subsequently, the number and type of test vectors necessary to achieve a given fault coverage and quality level improvement factor. The detection capability of the method to other types of catastrophic and parametric defects is also under investigation, as well as a statistical methodology based on cross correlation that will automatically distinguish between variations caused by process tolerances and those cause by defects.

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