Modeling Free Space Optoelectronic Interconnects

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Abstract

This paper presents a system level optoelectronic CAD tool, Chatoyant, which has been developed to meet the needs of mixed technology systems designers. We introduce component models and analysis techniques that enable our tool to support optoelectronic interconnect system design. We demonstrate these results with the analysis of two optoelectronic interconnection systems: a multi-channel high-speed link and a 1x2 optical MEM interferometer switch.

1. Introduction

We have created Chatoyant, a multi-level multi-domain CAD tool that has been successfully used to design and simulate free space opto-electronic interconnect systems [5][6][8][9].

Chatoyant is based on a methodology of system level architecture design. In this methodology architectures are defined in terms of models for "*modules*", the "*signals*" that pass between them, and the "*dynamics*" of the system behavior. For optical, electrical, and mechanical (O/E/M) systems, our *signals* are represented as electronic waveforms, mechanical deformations, and modulated carriers, i.e., beams of light. Using the characteristics of the O/E/M signals, we define *models* for the system components in terms of the ways they transform the characteristic parameters of these signals. Finally, we base the *dynamics* of the system behavior on a piece-wise linear time domain analysis of the propagation of the signals through the components.

A *4f*-optoelectronic link modeled in Chatoyant is shown in Figure 1. The center of the figure shows the system being modeled, a 3x3 VCSEL array propagating through a two-lens relay system to a 3x3-detector array. Across the top, we show the Gaussian beam profile of one beam of the array as it propagates through space. On the right, we show optical signals as they strike the detector array, while, on the bottom of the figure, we show a waveform and eye-diagram from one of the nine data

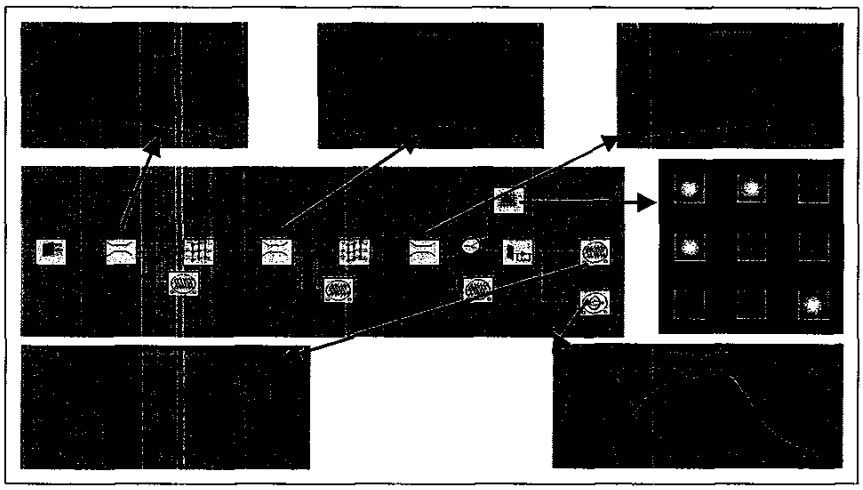

Figure 1 Chatoyant analysis of *4f* system

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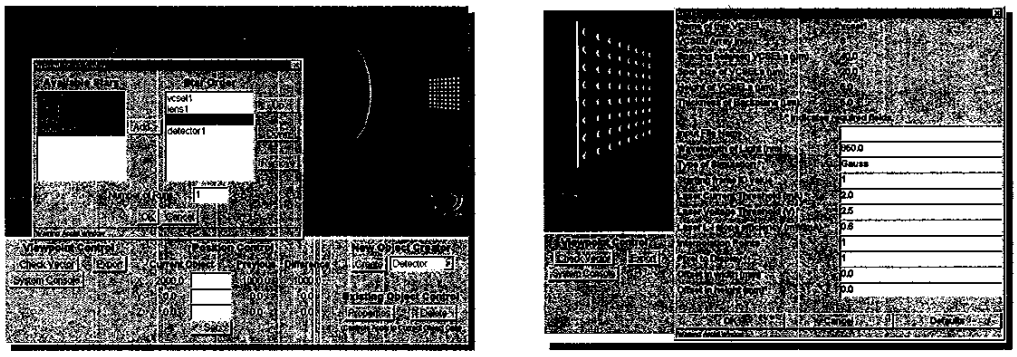


Figure 2 Chatoyant 3D graphical user interface

channels. The details of these analyses are explained later in this paper.

In the rest of this paper we present the features of Chatoyant that are useful in the modeling, simulating, and analysis of optoelectronic interconnects. We first present an overview of Chatoyant. Then, we discuss our modeling techniques for optoelectronic components that are used as building blocks in free space system design. We then focus on two example systems simulated with Chatoyant and present results that illustrate our model implementations and analysis techniques.

2. Chatoyant

Chatoyant is built upon the object-oriented simulation engine Ptolemy[2]. Chatoyant's component models are written in C++ with sets of user defined parameters for the characteristics of each module instance. The signal information is carried from module to module using a composite message type. The Ptolemy simulation method used in Chatoyant is called "Dynamic Data Flow" (DDF) with the modification that timing information is added to each message. This allows having multiple and run-time-rate variable streams of data flowing through the system, which is essential to support multiple domains.

As shown in Figure 1, in Chatoyant each icon represents a component model and the path of information between them is represented as lines. The models come from four component libraries. The Optical Library contains components such as lenses, lenslets, mirrors, and apertures. The Optoelectronic Library includes vertical cavity surface emitting lasers (VCSELs), multiple quantum well (MQW) modulators, and p-i-n detectors. The Electrical Library includes CMOS drivers and transimpedance amplifiers[4], and the Mechanical Library contains scratch drive actuators (SDA)[1] and other electrostatic devices.

Optoelectronic systems are composed of 3D objects where, unlike electronic systems, relative physical position matters. Therefore, we are developing an intuitive graphical user interface (GUI) Chatoyant3D. Chatoyant3D allows the user to choose from libraries of three-dimensional objects which can then be placed into a three dimensional "virtual world", as shown in Figure 2.

The advantage of using a web based 3D interface is that objects can be created and placed so that they match their real world counterparts. This results in a simpler,

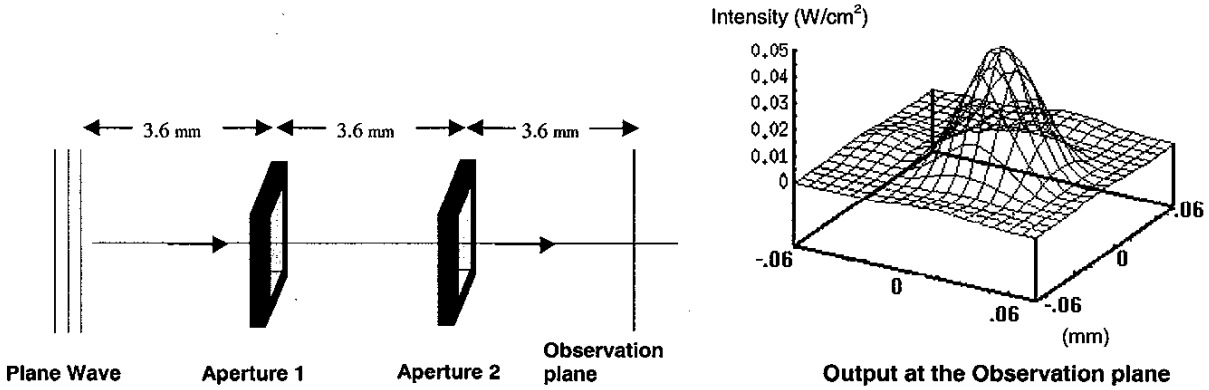
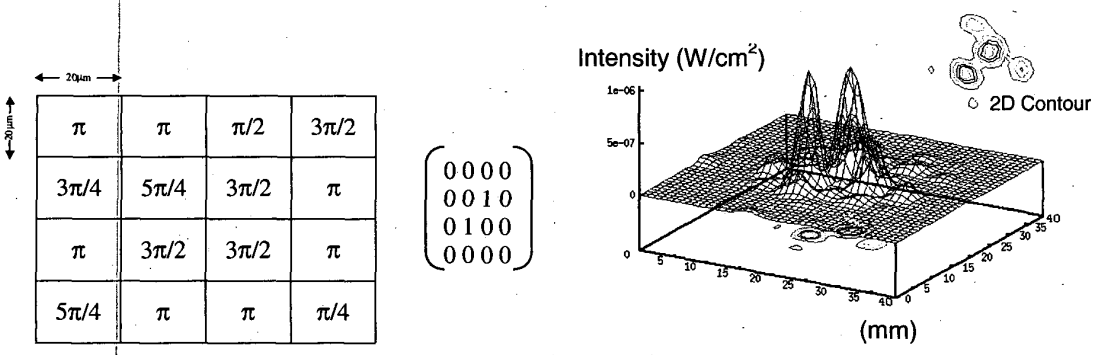


Figure 3 Plane wave propagation through cascaded apertures



(a) Phase mask **(b) On/Off matrix** **(c) Intensity profile**

Figure 4 Plane wave propagation through a phase mask

more intuitive interface. Further, this will allow platform independent remote use of Chatoyant running on a server compute engine.

2.1. Optical propagation models

Chatoyant uses geometric, Gaussian beam and Fresnel scalar approximations as optical propagation techniques [6][8]. For scalar propagation, the algorithm developed uses a computational efficient adaptive numerical integration routine to solve for the complex wave function at selected points. The wave front projected from each surface is interpolated and incorporated into the integration routine that solves for the pass through the next surface.

To illustrate our scalar propagation models, we show two examples. Figure 3 shows the normalized intensity plot of the output of a 850nm plane wave after passing through two cascaded 40x40μm apertures, where elements in the system are spaced by 3.6 mm. Figure 4 shows propagation of light through a 16 tile phase mask, which is shown in Figure 4(a). This mask has a tile size of 20x20μm and is used to produce the desired on/off intensity pattern, shown in Figure 4(b). The results are shown in Figure 4(c), where the observation plane is located 36 mm from the phase mask.

The computation time on a 400Mhz Pentium for the system in Figure 3 was under three minutes, while the time for computing the results of the phase mask was almost 45 minutes. This is because the phase mask acts as 16 independent sources.

2.2. Optoelectronic models

In this section, we introduce our methodology for modeling optoelectronic devices. Models for optical and mechanical components have been reported previously in [8][9] and [10].

Device characterization of an optoelectronic circuit module, in general, consists of a small to medium number of nodes. Typically, this consists of a group of lumped passive devices (R, C and L), which are extracted from distributed parasitic parameters, and a set of active devices. The active devices are characterized by differential equations where the values of parameters are dynamic. This representation is, in general, non-linear but can be modeled using a piece wise linear (PWL) technique. Linearizing the behavior of the non-linear devices by regions of operation simplifies the computational task to solve the system. This also allows us to trade accuracy for speed. PWL modeling offers reliable performance without the computational load of circuit simulators such as SPICE. Most importantly, PWL models for optoelectronic devices allow Chatoyant to integrate electrical and optical components in the same simulation.

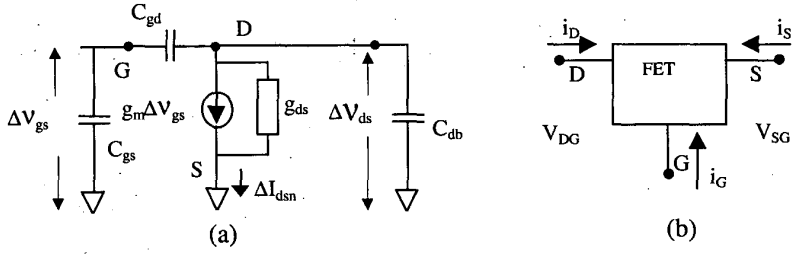


Figure 5 CMOS FET Model

Our modeling is accomplished in three steps. First, a Modified Nodal Analysis (MNA) matrix representation is created to characterize the device[13]. This gives us a complete matrix representation of the module.

Second, we perform linear and non-linear sub-block decomposition of the characteristic matrix representation. This gives a decomposition of the design into a linear multi-port sub-block section and non-linear sub-blocks. The linear multi-port sub-block can be thought of as characterizing the interconnection network while the non-linear sub-blocks characterize the active devices. The linear sub-block can be analyzed using a direct and exact solution. The solution from this block is a matrix in which elements correspond to the transfer function between a pair of input/output ports in the block. Thus, the passive component network between the active devices is fully characterized for any region of operation of the active devices.

Third, we perform piecewise modeling of the active devices for each non-linear sub-block. When we form each non-linear sub-block a MNA template is used for each device in the network. The use of piecewise models is based on the ability to change these models for the active devices depending on the changes in conditions in the circuit, and thus the regions of operations of each active device.

During each timestep in the simulation, the state variables in the module will change and might cause the active devices to change their modes of operation. Therefore, we re-compute and re-characterize the PWL solution caused by changes between piecewise models. This process is simplified using the transfer function between devices (given by the linear block pre-solution) as a guide.

2.3. Large signal models for CMOS devices

To illustrate our modeling of the active optoelectronic devices in module networks, we focus on CMOS transistors. Considering the classical model equations developed by Shockley [12] as characterizing the behavior of every device, a linearization of I_{ds} is performed using:

$$1)\Delta I_{ds} = g_m(P)\Delta v_{gs} + g_{ds}(P)\Delta v_{ds},$$

where P represents any point of operation for the device. Transconductance (g_m) and conductance (g_{ds}) are the parameters characterizing the device.

The piecewise linear approximation shown in Figure 5(a) was developed using Equation 1 to characterize a basic CMOS transistor with the proper combination of linear parameters in the MOS transistors as well as the additive effects of parasitic capacitances.

In this figure, g_m and g_{ds} represent the effective transconductance and conductance in the transitor, while I_{dsn} represents the drain current.

Rather than capturing this model directly, in order to include this device in the matrix representation we use the three port network representation, shown in Figure 5(b), defined using the transfer function between every pair of nodes in the model. This MNA formulation allows incorporating the FET as a three-port element into the MNA of a complete optoelectronic module. The non-linear nature of the FET is modeled by piecewise changes in values of the parameters (g_{ds}, g_m, C_{ds}, C_{gs} and C_{ds}) depending on the region of operation and are thus functions of V_g,V_d, and V_s.

Understanding that the degree of accuracy of piecewise linear models depends mainly on the step size chosen for the time base, an adaptive control method for the time steps is added to the models[3]. A binary search over the time step interval is the basis for this dynamic algorithm. The algorithm discards non-significant samples, which do not appreciatively affect the output, and adds samples when the output change is greater than a user defined tolerance. The inclusion of the samples during fast transitions or suppression of time-points during "steady state" periods optimizes the number of events used in the simulation.

2.4. Electrical simulation tests

To show the speed and accuracy of our models, we performed several experiments comparing our results to that of Spice 3f4 (Level II). The test was a multistage amplifier with a significant number of drivers. PWL models with a fixed sampling rate and PWL models with an adaptive sampling rate (PWLA) were tested versus Spice at 10, 100, 500 and 1000 MHz.

Table 1 and Figure 6 show that the speed up achieved for the same number of timepoints is at least two orders of magnitude faster than Spice. It also shows that the adaptive algorithm for time step control (PWLA) effectively reduces the execution time compared to PWL models alone. The adaptive algorithm also improves the stability of the model. PWLA is able to give solutions to the system even where the PWL fails. This test also shows that the efficiency of both models in this range is independent of the frequency of operation.

These results show that the models are well suited to

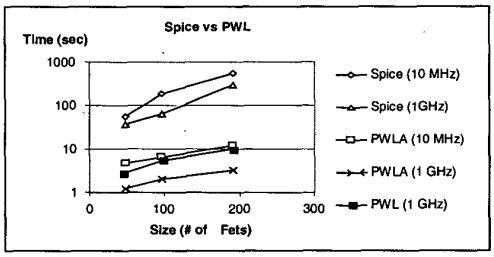


Figure 6 Spice vs. PWL and PWLA models in a system of multiple FETs (f=100/500/1000 MHz).

	f= 10 MHz C=3.774ff			f= 100 MHz C=3.774ff			f= 1 GHz C=3.774ff		
	SPICE	PWLA	PWL	SPICE	PWLA	PWL	SPICE	PWLA	PWL
Speed									
Time(secs)	0.13	0.093	0.15	0.12	0.089	0.091	0.12	0.094	0.089
Iterations	307	100	200	313	100	100	300	100	100
Accuracy	0	9.1%/18.8 SD	1.8%/4.7 SD	0	3.4%/6.8 SD	3.3%/6.7 SD	0	10%/12.9SD	9.99%/13.8SD

Table 1 PWL simulation performace

perform accurate and fast simulations for the typical multistage CMOS drivers and transimpedance amplifiers widely used in optoelectronics applications.

3. Simulation and analysis examples

In this section we show how Chatoyant can model and simulate complete optoelectronic interconnect systems. The first set of systems is based on the *4f* VCSEL array link presented above. The second system is a dynamic optical micro-mechanical-electrical system (MEM) used for mechanical switching of arrays of optical data.

3.1. High speed parallel link

A complete optoelectronic simulation of a *4f* optical communication link is presented in Figure 7. The top half of the figure shows the system as represented in Chatoyant. Each icon represents a component model, and each line represents a signal path (either optical or electrical) connecting the outputs of one component to the inputs of the next. Several of the icons, such as the VCSELs and receivers, model the optoelectronic components themselves, while others, such as the output graph, are used to monitor and display the behavior of the system. The input to the system is a signal with speed varying from 300MHz to 1.5GHz.

A Gaussian noise with variance of 0.5V has been added to the multistage driver system to show the ability of PWL models to respond to arbitrary waveforms. In the figure, several snapshots show the behavior of the CMOS drivers under a 300MHz noisy signal. Noise with levels over the threshold cause an effective change in state in the inverter. It is interesting to make three observations from the figure: the difference in amplifications in the noise depends on the output level, the immunity to noise and recovery of the signal due to the inverter CMOS sections, and the clipping of negative noise spikes in the source because of the VCSEL threshold.

The three eye diagrams, shown in Figure 7, (at 300MHz, 900MHz, and 1.5GHz) denote the effects of frequency on the quality of the received signal. For the component values chosen the system operates with reasonable BER up to about 1GHz. Of course, many factors affect this performance and by making different assumptions on component values we can show systems with arbitrarily good (or poor) performance. Our goal

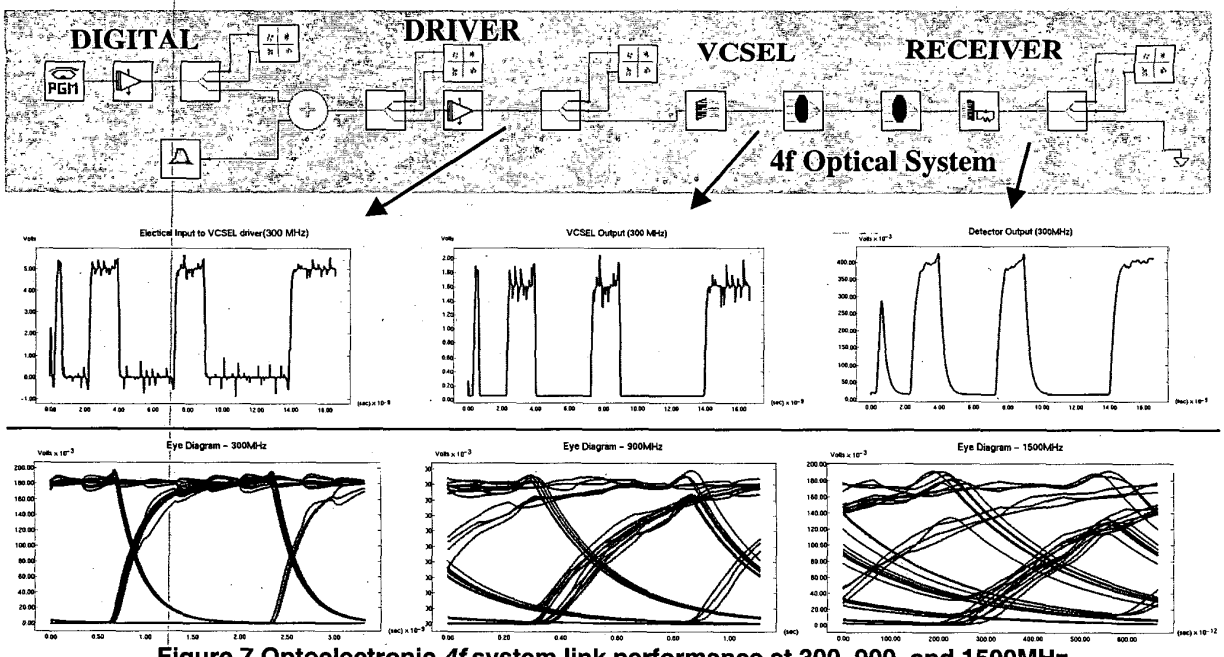


Figure 7 Optoelectronic *4f* system link performance at 300, 900, and 1500MHz

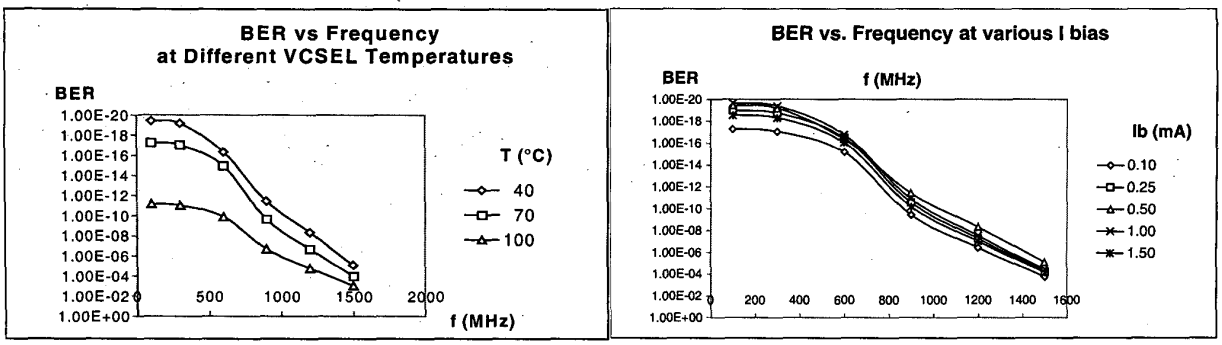


Figure 8 System performance

here is not to model a particular real system, but to show how we can model a variety of systems, with different component values.

For this *4f* system, the VCSEL and driver circuits explicitly model the effects of bias current and temperature on the L-I efficiency of the lasers. Figure 8 shows the effects of temperature, *T*, and current bias, *Ib*, on the BER of the link. Generally, the frequency response of the link is dominated by the design of the receiver circuit, however it is interesting to note that both the VCSEL temperature and bias have a significant effect on system performance, due to their impact in the power through the link. Perhaps most interesting is the fact that increasing bias current does not always correspond to better performance over the whole range of frequencies examined. Note that the curve for 1mA bias offers the best performance below 600MHz, however the 0.5mA bias (the nominal threshold of the VCSEL), crosses the curve for 1mA and achieves the best performance at higher frequencies.

3.2. 1x2 Optical switch

Our second example system is a 1x2 optical interferometer switch shown in Figure 9. For our 1x2 switch, a 3x3, VCSEL array source is split into two beam arrays, providing inputs into two interferometers. Both interferometers (beam splitter, mirrors, and beam recombiner) are boxed by a dashed line in Figure 9. A movable plate on the substrate of the wafer holds two of the mirrors from each path in the shape of an "X". The position of the plate is controlled by feedback circuitry in the system, and is moved by two sets of MEM scratch drive actuators (SDA)[1], shown by the lined rectangular

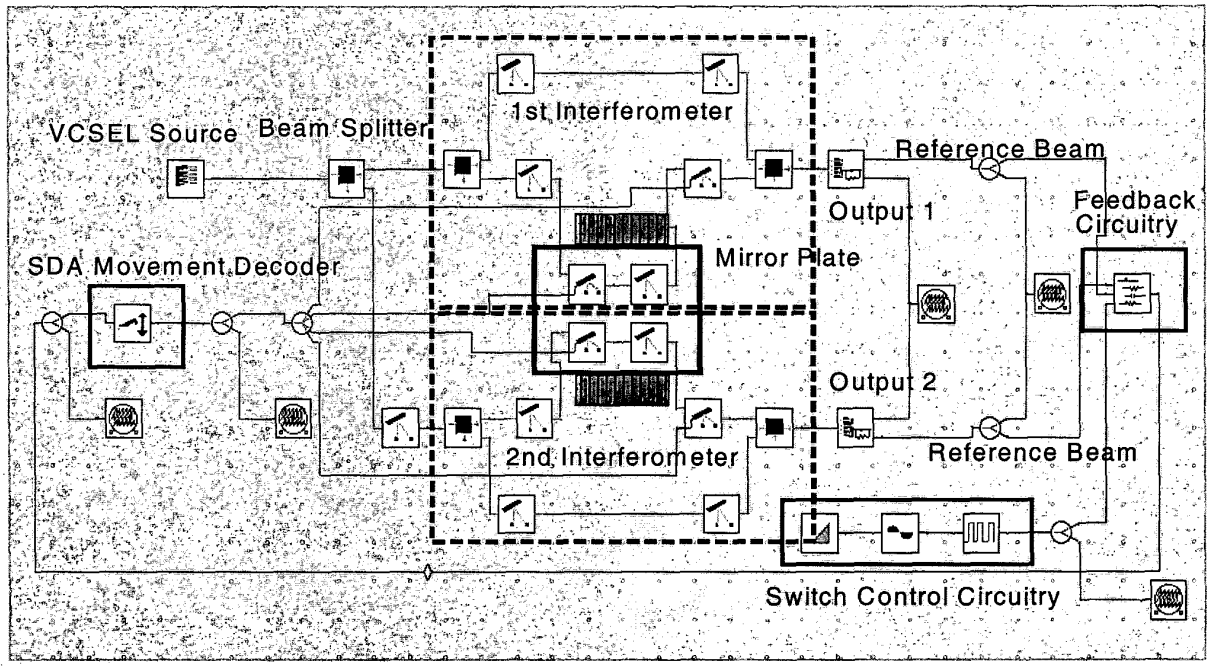
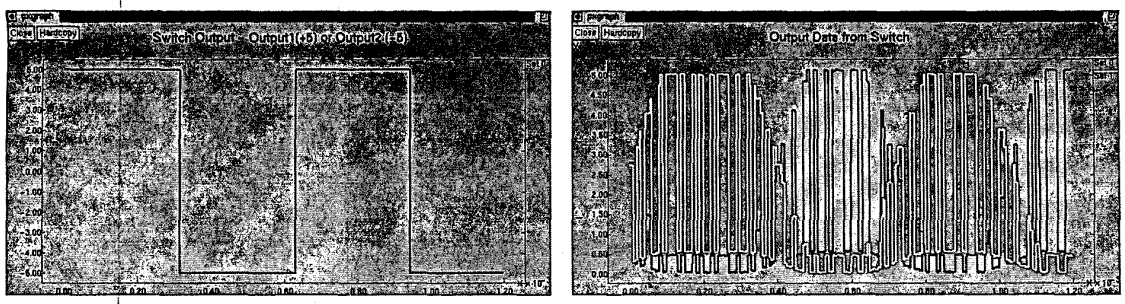


Figure 9 1x2 Interferometer switch



(a)Switch Control Voltage (b)Data Beams

Figure 10 Dynamic simulations of 1x2 interferometer switch

boxes. The SDA sets move the mirror plate back and forth controlling the optical path lengths of one beam in each interferometer. This effect is inverse in each device, while the optical path length of one interferometer is shortened causing constructive interference on one detector, the other optical path is lengthened, causing destructive interference. The plate and the SDA are not directly drawn in Chatoyant, since they are modeled as signals altering the optical paths. We have added them to the figure for clarity. The components are created using surface micromachined technology[14]. With this technology, free-space micro-bench components can be fabricated "out of plane", or normal to the surface, and pre-aligned during the fabrication of the devices, and post-aligned with micro-positioners.

The SDAs are modeled in Chatoyant by the actuator's "step" size (determined by the height and length of the actuator) and the voltage pulse train, which drives the actuator. Two set of actuators are needed to move the mirror plate, one for each direction, and are controlled by electronic feedback circuitry that specifies which actuator, if any, should crawl. Since we are using a 3x3 array of VCSEL sources, one beam is used as a reference and is always "on". This beam is detected and compared with the desired value in the feedback circuitry. The other 8 beams are used for data transfer. The feedback circuitry is a basic comparator, which compares the converted voltage from the designated detector with a threshold voltage, specified by the user. If the received voltage is not at the desired level, the actuator keeps moving the mirrors to a position that produces the correct interference, resulting in the correct optical power at the desired detector.

For Detector 1, Chatoyant reports a worst case static efficiency of approximately 56% for one of the beams in the array. 23% of the power is lost due to the efficiency of the mirrors, and an additional 21% of the power is lost due to the beams' divergence and the detector sizes. With the longer optical propagation and the extra mirror, Detector 2's efficiency drops to approximately 41%. The detector sizes and spacing also generate optical system crosstalk. Worst case crosstalk between neighboring detectors is measured at -15.5 dB.

Assuming, through standard MEM fabrication, that each mirror could be fabricated within a tolerance of +1.0 degrees of its ideal position. Using uniform distributions on the mirror angles, Chatoyant's Monte Carlo analysis of the system for 10,000 samples shows the average system efficiency on Detector 1 is approximately 40%, compared to the maximum of 56%.

As with the *4f* system above, we simulate streams of data passing though the switch to the specified detectors. Figure 10 shows two outputs from a single simulation of the switch in Chatoyant. Figure 10(a) shows a 1.6 kHz square wave, which selects the switch's output. When the value is positive, Output 1 is selected, and when the value is negative, Output 2 is selected. The optical detectors are composed of p-i-n photo diodes, which convert optical power into current, and a transimpedance amplifier, which convert the current to voltage. Figure 10(b), shows one stream of data that is passed from one VCSEL source, through the interferometers, to the desired switch output. Both outputs from the switch are shown in the same graph, the first output by a solid white line, and the second output with a solid black line. In these simulations, the noise parameters were exaggerated for illustrative effects on such a slow running system. In this example, the optical data stream is running at only 125 kbits/sec. In a real application, the optical signal would actually be at a much higher bit rate (300 MHz - 3 GHz), but is kept slow here for illustration purposes. In this example, for each switching pulse, approximately 50 bits are passed through to the receiver. In reality, we would switch packets of 10^3 - 10^5 bits. Similarly, we show data bits during the switch transition, while in real systems "guard bands" would be added to the data stream.

In theory, with a 50 kHz clock driving the SDAs, the actuators will take 10 μsec to move each of the 11nm steps. With a 850 nm laser source, the optical paths in the interferometer differ by 212.5 nm between complete constructive and destructive interference. For worst case switching time, the movable mirror plate, would have to move this entire distance. With a step size of 11nm, this

would take approximately 20 steps, resulting in a switching time of 200 μsec.

However, in simulation, we find that with the detector parameters and the feedback circuit voltage reference specified, the maximum number of steps the SDA is moving is only 12, resulting in a switching time of 120 μsec. This is because neither total constructive or destructive interference is achieved. This is visible in Figures 12(b), with the "off" switch output not completely reaching 0 volts. Total interference could be reached at the cost of increased switching time, by altering the feedback circuitry parameters.

Using parameters from the published literature, the free space interferometer switch that we have modeled here is comparable to optical fiber switches built by Lee and Marxer. Worst case switching time of Lee, et al.'s[7] surface-micromachined, moving plate mirror, fiber switch was found to be between 10 and 15 msec, and Marxer et al.[11], using bulk-micromachining and a comb-drive reports a switching time of 200 μsec.

Using Chatoyant's BER analysis, the designer can perform trade-offs between BER, switching time, and mechanical tolerancing to achieve the desired system performance. With a switching time of 120 μsec and exaggerated noise parameters (with a total variance of 0.18), we calculate the BER of the system to be $2.7*10^{-30}$. However, an interesting trade-off can be found between the switching speed and the BER of the system. If we reduce the switching time by decreasing the threshold voltage of the comparator, the SDAs do not move as many steps, however, the BER of the system increases.

4. Summary and Conclusions

Multi-domain modeling and multi-rate simulation tools are required to support mixed technology system design. This paper has shown Chatoyant's support for simulating and analyzing free space interconnection systems with models for optical, electrical, and mechanical models for components and signals. By providinging a variety of modeling techniques (analytic, empirical, and surface-response) and multiple abstraction levels, Chatoyant has the ability to perform and analyze optical, electrical, and mechanical trade-offs which makes it valuable to optoelectronic system designers. Keeping simulations, along with analysis techniques such as Monte Carlo for mechanical tolerancing, BER, crosstalk, and insertion loss, within the Chatoyant framework allows for quick and efficient analysis throughout multiple domains.

Acknowledgments

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