Characterization of CMOS Defects using Transient Signal Analysis

James F. Plusquellic[1], Donald M. Chiarulli[2] and Steven P. Levitan[3]

[1]Department of CSEE, University of Maryland, Baltimore County
[2]Department of Computer Science, University of Pittsburgh
[3]Department of Electrical Engineering, University of Pittsburgh

Abstract

We present the results of hardware experiments designed to determine the relative contribution of CMOS coupling mechanisms to off-path signal variations caused by common types of defects. The transient signals measured in defect-free test structures coupled to defective test structures through internodal coupling capacitors, the power supply, the well and substrate are analyzed in the time and frequency domain to determine the characteristics of the signal variations produced by seven types of CMOS defects. The results of these experiments are used in the development of a failure analysis technique based on the analysis of transient signals.

1.0 Introduction

Transient Signal Analysis (TSA) [1] is a defect detection technique for digital CMOS devices that is based on the analysis of transient signal behavior. The method analyzes the voltage transient waveforms measured simultaneously at multiple test points while a logic signal transition is applied to the primary inputs. These transient waveforms characterize the physical components of the coupling network in a digital device. Variations in the transient signals across different devices are a direct consequence of changes in the resistive, inductive and capacitive components of the coupling network, as well as in the gain and threshold voltage characteristics of the transistors. Variations in the values of these circuit parameters may result from process tolerance effects, or they may result from defects.

In previous work, we demonstrated that it is possible to detect defects by analyzing the small signal variations at test points that are not on logic signal propagation paths from the defect site [2][3]. We indicated that this is possible because of the coupling mechanisms that exist in CMOS devices, namely the resistive and capacitive coupling through the power supply and the wells, as well as the parasitic capacitive and inductive coupling between conductors. These mechanisms couple the large signal variations of faults at defective nodes to adjacent conductors where they can be measured as small signal variations at test point nodes.

We also demonstrated that by cross-correlating the signals measured simultaneously at different topological locations on the device, it is possible to distinguish between signal variations caused by process tolerance effects and those caused by defects [4]. This is true because process tolerance effects tend to be global, causing signal changes on all test points of the device. In contrast, signal variations caused by a defect tend to be regional and more pronounced on test points closest to the defect site.

In this paper, we present some preliminary data which suggests the applicability of TSA to failure analysis. Failure analysis is the process of determining the physical defect that causes a component failure [5][6][7]. It includes an analysis of both the defect type and the location [8][9]. In this research, we show that it is possible to characterize defect type by analyzing the transient signals of the defect in a test device which we designed. In our experiments, we introduce seven types of shorting and open defects [10][11] into test structures and analyze the variations in the signals measured both on the defective test structures and on non-defective test structures, which are coupled to the defective test structures through one or more coupling

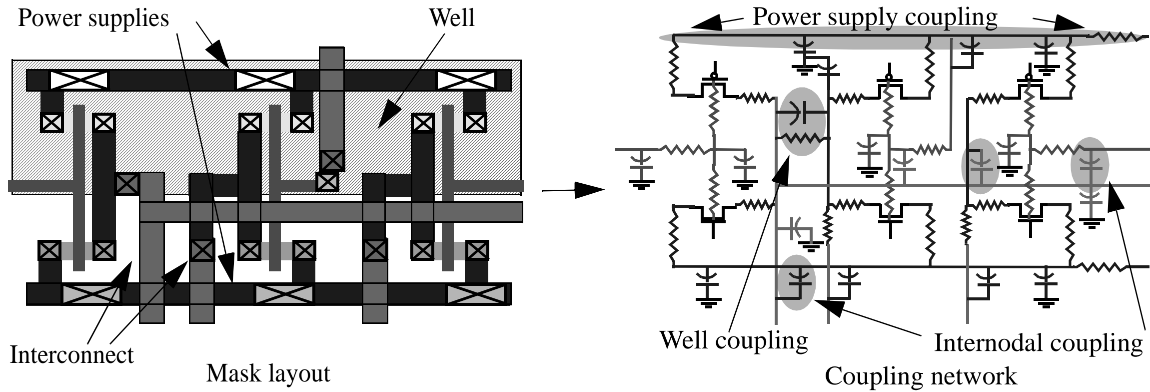

Figure 1. CMOS coupling mechanisms.

mechanisms. We analyze the signal variations of the coupled test structures in both the time and frequency domain and show that it is possible to distinguish between the various defect types by interpreting these signals.

The relative contribution of each of the coupling mechanisms to the off-path signal variations is also examined in our experiments. The four primary coupling mechanisms include power supply, internodal, well and substrate [12]. Examples of these coupling mechanisms are shown shaded in the RC model of a CMOS mask layout of Figure 1. We show that the predominant coupling mechanism is the power supply but also show that n-well coupling produces measurable variations. In addition, we show that internodal and p-well coupling, though measurable, are much less significant than the power supply and n-well coupling mechanisms.

The remainder of this paper is organized as follows. In Section 2, we describe the structure of the test device and experimental setup. In Section 3, we analyze the waveforms from hardware experiments conducted on devices with intentionally inserted shorting and open defects. Section 4 gives a summary and conclusions.

2.0 Experiments

In order to generate transient signals for each of the defects under study, we designed a chip with three arrays of test circuits which included both defect-free and intentionally defective structures. We also included an input control system that allowed each of the elements of the arrays to be examined individually. The three arrays implemented test circuits for a single inverter, a nand gate and a pair of cascaded inverters. The test structures within each array were implemented with identical topologies.

Within each array are eight test macrocells; a defect-free reference macrocell and seven defective macrocells into which one of seven defect types is introduced. In each macrocell, there are five cells composed of paired test structures (gates) that are identical except for the coupling architecture. The first test structure of the pair is driven with the input stimulus and the other is coupled to it through one or more coupling mechanisms. In this way, we control both the defect type and coupling architecture in different combinations across forty experiments in each of the three arrays. The input control logic allows each of these cells to be examined individually without interference from signal crosstalk.

Four devices of the experimental design were fabricated at MOSIS using ORBIT’s 2.0 micron SCNA process. A digitizing oscilloscope with a bandwidth of 1 GHz was used to collect a 5120 point waveform from each of the test points. The averaging function of the oscilloscope was used to reduce ambient noise levels. The measurements were taken on twenty micron metal 2 squares at a probe station using a PicoProbe, model 12C, with a 100 FF and 1 MOhm load. The test structures were stimulated with a 50% duty cycle square pulse at 5 MHz.

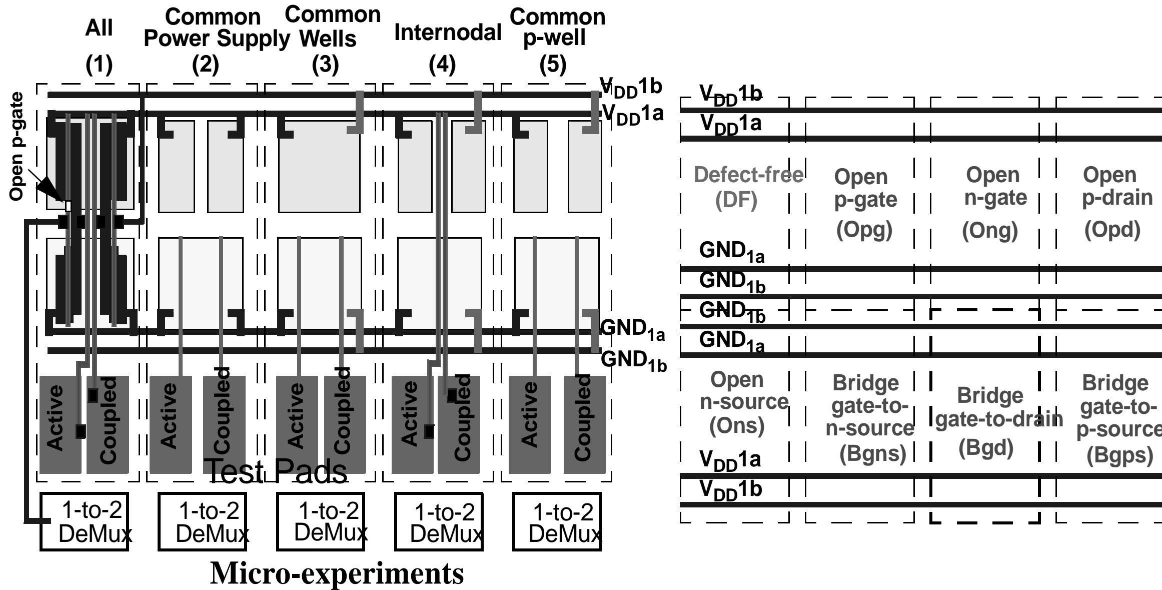

Figure 2. Five cells of a macrocell showing sensitized and coupled inverter pairs.

Figure 3. INVERTER array macrocells.

2.1 Experimental device layout

Figure 2 shows the layout of an Open p-gate macrocell in which the five cells are shown tiled horizontally. The left-most cell consists of an inverter pair that is replicated across the forty experiments in this array. A two micron square of poly is shown removed from the gate driving the p-type transistor of the left inverter in the pair. Although the inverter pairs of cells 2 through 5 are not shown, the open defect is introduced into the inverters of these cells as well. The right inverter of each pair is defect-free and held at a steady-state logic 1 output. The *1-to-2* demultiplexer shown along the bottom of the figure delivers the stimulus to the input of the defective inverter.

We left out the inverters in cells 2 through 5 in Figure 2 in order to emphasize the differences in the coupling architecture across the set of five experiments. The inverter pair in cell 1 (labeled 'All') are coupled through the four primary coupling mechanisms, power supply, well, internodal and substrate. For example, the supply terminals of both inverters are tied to common V_{DD}1a and GND_{1a} rails, both inverters have common n-well and p-wells and the outputs of both inverters run parallel to each other in poly at minimum spacing. Cells 2, 3 and 4 systematically remove two of either the n-well, power supply or internodal coupling mechanisms. Cell 5 removes all coupling mechanisms except p-well and substrate. In fact, the p-well is common across all five cells since the entire substrate is doped p-type in an n-well technology. Therefore, we can not measure the coupling effects of substrate only. However, by subtracting the waveforms of cell 5 from those of cells 2 and 4, the coupling effects due to the p-well are removed, isolating the coupling effects due to the power supply and internodal coupling capacitors.

Two test pads are shown for each cell along the bottom of Figure 2. The test pad of the left inverter, labeled **Active**, permits the response characteristics of the test inverter to be measured directly. Since the input of the coupled inverter on the right is held in steady state, the **Coupled** test pad measurements capture only the signal variations that couple from the test inverter on the left.

Figure 3 shows the layout of the INVERTER array. Eight macrocells are shown, one macrocell contains defect-free test structures while the remaining seven contain defective test structures that are identical except for the defect type. The defect-free macrocell is used as the reference. The macrocells with open defects contain inverters with open p-gates (*Opg*), open n-gates (*Ong*), open

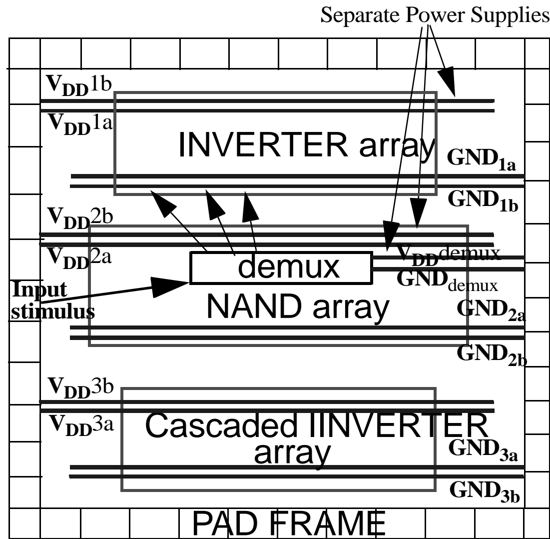

Figure 4. Block-level diagram of the test device.

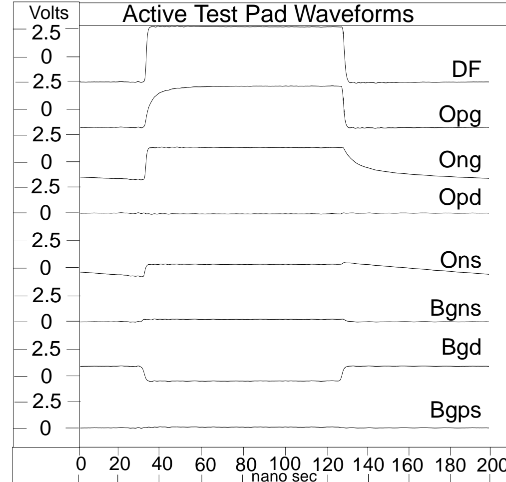

Figure 5. Active test pad waveforms of cell 1 of the eight macrocells.

p-drains (*Opd*) and open n-sources (*Ons*), respectively. The macrocells with bridging defects contain inverters with gate-to-n-source (*Bgns*), gate-to-drain (*Bgd*) and gate-to-p-source (*Bgps*) resistive shorts.

The open defects were created in the inverters of macrocells *Opg* and *Ong* by removing two micron squares of poly and, in the *Opd* and *Ons* inverters, by removing three micron squares of Metal 1. Poly was used to create resistive shorts in the *Bgns*, *Bgd* and *Bgps* inverters with resistances of approximately 270 Ohms, 500 Ohms and 525 Ohms, respectively.

Figure 4 shows a block diagram of the test device. The three arrays are labeled INVERTER, NAND and Cascaded INVERTER to identify the topology of logic under test in each array. The effects of circuit topology will be evaluated in future work by comparing the INVERTER experiment results reported here with measurements taken from the NAND and Cascaded INVERTER arrays.

A *1-to-20* demultiplexer, shown centered in the diagram of Figure 5, is used to direct the input stimulus to one of twenty *1-to-2* demultiplexers within each of the arrays, and then on to one of the forty cells. The twenty output lines of the *1-to-20* demultiplexer fan out to three *1-to-2* demultiplexers (not shown) in each of the three arrays. In order to prevent crosstalk between the test structures in different arrays, separate power supplies are used. The NAND and Cascaded INVERTER arrays were powered off for the INVERTER experiments by holding V_{DD}2a, V_{DD}2b, V_{DD}3a and V_{DD}3b at GND.

3.0 Waveform Analysis

In this section, we analyze the waveforms measured from the Active and Coupled test pads of the INVERTER array. We demonstrate that it is possible to distinguish between different types of open and shorting defects using signals measured at nodes coupled to the defective node through one or more coupling mechanisms. The waveforms measured on the Active test pads are analyzed first. References to these results are made in the analysis of the Coupled test pad waveforms in order to explain the observed behavior.

3.1 Active test point waveform analysis

The Active test pad signals from cell 1 of each macrocell are shown in Figure 5. For example, the top-most waveform is the Active test pad signal measured from the first defect-free reference cell in macrocell *DF*. The waveforms shown below it were measured from the cell 1 Active test

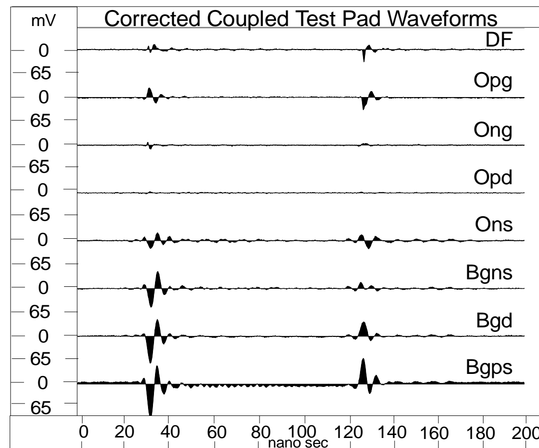

Figure 6. Corrected Coupled test pad waveforms of cell 1 of eight macrocells.

pads of the seven defective macrocells. It is notable that each of the waveforms in the figure are DC offset at -2.5V because the measurements were taken with the probe AC coupled to the amplifier. Although this was effective in eliminating DC drift in the probe's power supply, it makes it difficult to determine the absolute output voltage range of the test pad signals.

There are several important features in these waveforms that will be revisited in the analysis of the Coupling waveforms:

- *Opg*: The *Opg* waveform switches over 4V with a slowed rising transition indicating that the floating p transistor of the defective inverter is pseudo-stuck-on. Due to the sharpness of the edge, it is likely that the gate has floated to a value close to GND. The delay in the defect-free waveform's rising transition is 1.3ns while the *Opg* waveform requires 13ns to reach 90% of its output voltage and 1.8ns to reach its midpoint voltage.
- *Ong*: The *Ong* waveform switches over 3V with a slowed falling transition indicating that the floating n transistor of the defective inverter is pseudo-stuck-on. The falling transition is somewhat slower when compared to the rising transition of the *Opg* waveform, which indicates that the floating gate voltage is closer to the threshold voltage than the floating gate of the *Opg* macrocell inverter. The falling transition requires 30ns to reach 90% and 4.2ns to reach its the midpoint voltage.
- *Opd*: The *Opd* waveform is stuck-at 0. Closer inspection reveals that it switches over a 50 millivolt range.
- *Ons*: The floating output in the defective inverter slowly falls from 5V to 3.8V, which may be caused by the reverse-biased leakage current of the n-transistor source and drain.
- *Bgns*: The low resistances of the poly in the *Bgns* cells prevent the 1-to-2 demux from switching the input of the defective inverter, resulting in an output stuck-at-1 condition.
- *Bgps*: The low resistance in the *Bgd* experiment created a condition in which the output of the 1-to-2 demux overpowered the drive capability of the inverter's transistors. The *Bgd* inverted waveform swings over a 1.3V range.
- *Bgd*: Same as *Bgns* except that the output is stuck-at-0.

The Active test point waveforms from cells 2 through 5 of each macrocell exhibit behavior that is very similar to the behavior described for the cell 1 waveforms. Differences in the worst case are less than 500ps along the x axis and less than 100 millivolts along the y axis. The high degree of correlation in the waveforms of the identically configured test structures supports our expectation that intra-device process tolerances are very small. Similar experiments on the other three devices are currently underway. This additional data will permit a more extensive evaluation of intra-device process tolerance effects and a comparison to be made with inter-device process tolerance effects.

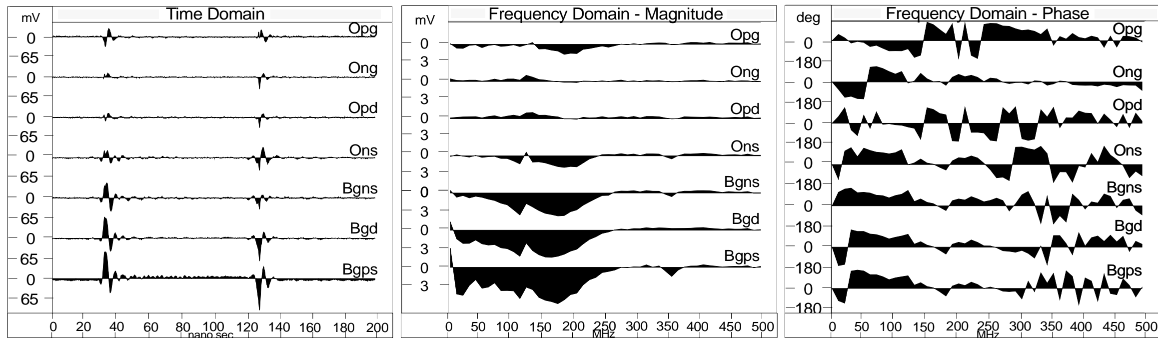

Figure 7. Time, Magnitude and Phase SWs from Cell 1: All coupling mechanisms.

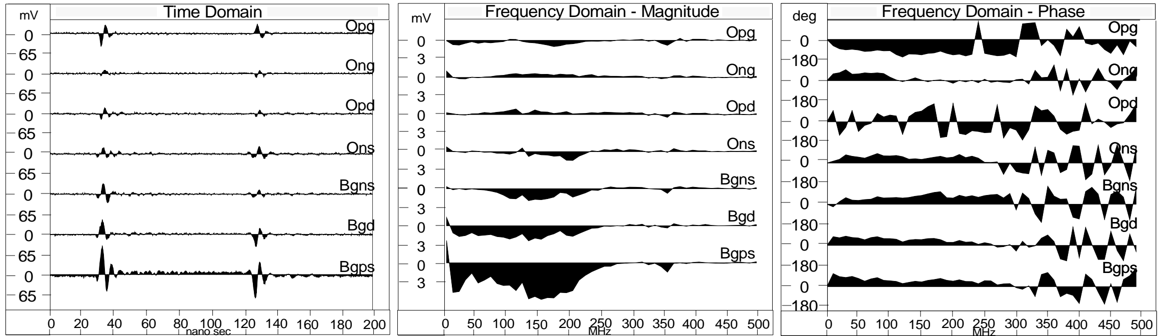

Figure 8. Time, Magnitude and Phase SWs from Cell 2: Power Supply Coupling.

3.2 Coupled test point waveform analysis

Figure 6 shows the waveforms collected from the Coupled test pads of cell 1 of the eight macrocells. Thirty-two samples of the test pad signals were averaged to reduce ambient noise levels. In addition, these waveforms were corrected for electromagnetic coupling (EMC) using a set of reference waveforms. The EMC generated by the input termination network and package wires was removed by subtracting the reference waveforms from the coupled waveforms. The corrected waveforms shown in the figure are shaded along a zero baseline to emphasize the variations introduced by the coupling mechanisms.

We prepare the waveforms shown in Figure 6 for analysis by creating Signature Waveforms or SWs. Signature Waveforms are designed to highlight the differences in the signal behavior of the defective macrocells with respect to a defect-free reference waveform. Specifically, the time domain SWs on the left of Figure 7 were created by subtracting the seven defective macrocell waveforms from a defect-free reference waveform labeled *DF* in Figure 6. The Magnitude SWs of Figure 7 are created by first performing a discrete fourier transform on the waveforms of Figure 6 and then computing difference waveforms from the magnitude components. A similar procedure is used to create the Phase SWs except the values are adjusted to capture the relative phase shift from the reference.

The SWs shown in Figures 7 and 8 are distinguishable across the seven macrocell experiments in one or more of the Time, Magnitude or Phase domains. Defect characterization is more difficult in Figures 9 through 12 in which power supply coupling has been removed. It is also true that the Time and Magnitude SWs of Figures 7 and 8 more accurately reflect the signal behavior of the Active test pad waveforms than the SWs in Figures 9 through 12. In particular:

- *Opg*: We noted a delayed rising transition in the Active test pad waveform of the *Opg* macrocell in Figure 5 indicating the p-channel transistor remained in a pseudo-on state. The *Opg* Time Domain SW shown in Figure 7 captures the transients caused by the shorting (and un-shorting) condition across the inverter at both the rising (30ns) and falling (130ns) edges. The waveform subtraction operation has removed the symmetry in the SW at the transition

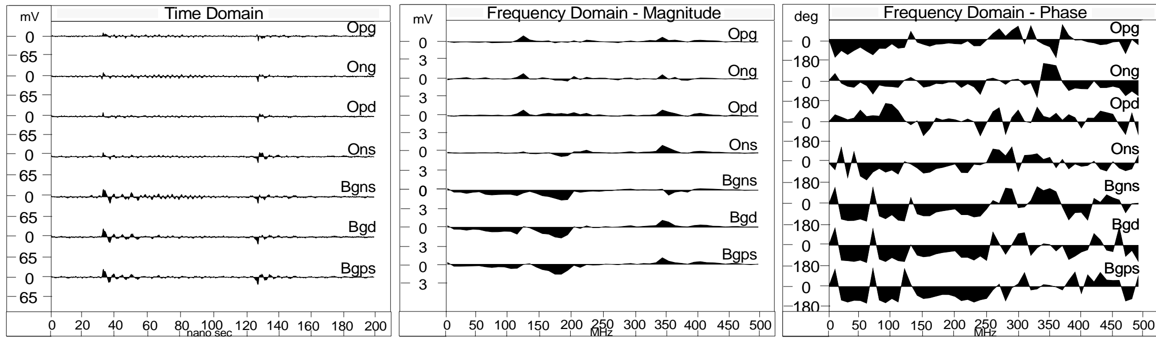

Figure 9. Time, Magnitude and Phase SWs from Cell 3: p and n Well Coupling.

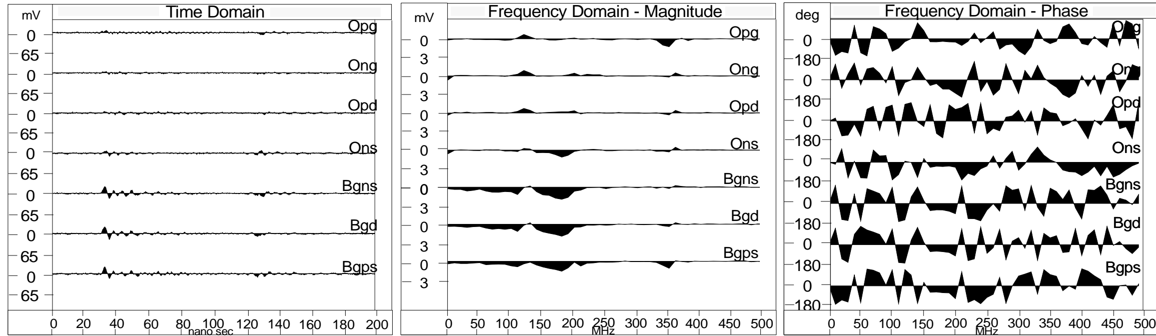

Figure 10. Time, Magnitude and Phase SWs from Cell 3 minus Cell 5: n Well Coupling.

regions that is more evident in the coupled waveform of Figure 6. Figures 8 through 12 supports the fact that the coupling occurs primarily through the power supply. The Magnitude and Phase SWs also show distinguishable characteristics particularly among the Phase SWs of Figures 7, 8 and 9.

- *Ong*: The *Ong* SW illustrates a different condition for Open n-gate macrocell experiments. Similar to the *Opg* experiment, a shorted condition exists but the slower transition (30ns verses 13ns) at the falling edge and the smaller output voltage range (3V verses 4V) of the defective inverter has reduced the transient at the rising and falling transition. This is most apparent in the back edge transient of the *Opg* Time Domain SW which is nearly identical to the defect-free back edge transient of Figure 6. With regard to the frequency domain, the Phase SWs of Figures 7 and 8 are easily distinguishable from the other SWs in the figures.
- *Opd*: The stuck-at 0 condition at the output of the defective inverter in the *Opd* macrocell experiments and the subtraction operation creates an *Opd* Time Domain SW that is almost identical to the *DF* coupled waveform of Figure 6. It is important to realize that this condition does not prevent this type of defect from being detected. This is true because the patterns of other defect-free inverter SWs would be baseline (no pattern) or characterized by process tolerance effects. In either case, we would not expect to obtain SWs that are similar to those shown for *Opd* in the Time, Magnitude or Phase domains. Similar to the results of the *Opg* and *Ong* experiments, the Phase SWs of Figures 7 through 9 are more distinctive than the corresponding Time or Magnitude SWs.

Since the *Opd* Time Domain SW is the image of the defect-free coupled waveform, it is possible to examine the contributions of the coupling mechanisms in the defect-free case indirectly using the set of *Opd* SWs in Figures 8 though 11. From these SWs, it is evident that more than one coupling mechanism is responsible for the transients. For example, Figure 8 portrays the transient as a sinusoid on the back edge. The leading downward spike on the back edge of the *DF* waveform of Figure 6 is created by internodal and p-well coupling mechanisms as indicated in Figures 11 and 12.

- *Opg*: The *Ons* Time Domain SW of Figure 7 shows an unusual amount of transient activity

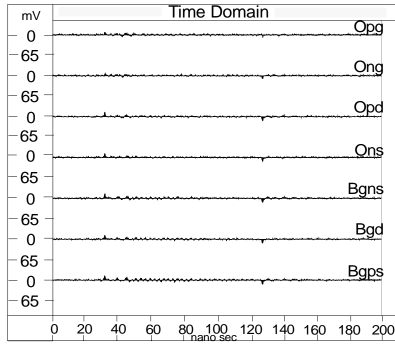

Figure 11. Time domain SWs from Cell 3: Internodal Coupling.

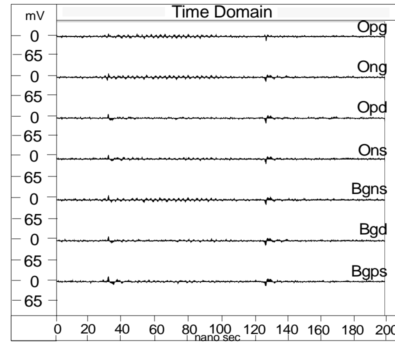

Figure 12. Time domain SWs from Cell 5: p Well Coupling.

given that the output of the defective inverter only swings over 1.2V range. The additional transient activity at the rising transition may be due to the charging of the additional n-diffusion source capacitance. Similar to the *Opg*, the primary coupling mechanisms appears to be the power supply but Figure 9 indicates that the wells also contribute to this variation, particularly on the back edge. Unlike the observations made in the previous experiments, the Phase SWs of Figures 7 and 8 below 250 MHz are very similar to the Phase SWs of the *Bgd* and *Bgps* experiments. However, the Magnitude SWs in these figures are easily distinguished across the experiments.

- *Bgns*: The *Bgns* Time Domain SW is distinguishable from the *Bgd* and *Bgps* SWs primarily on the back edge. It should be noted that the short in all three cases is between the demultiplexer supply rails and the inverter supply rails. In particular, the output of the demux is shorted to ground in the cells of the *Bgns* macrocell. Since the output does not switch, the short holds the output state of the demux near GND. It is not clear why the return-to-zero state transition of the demux causes a larger transient than the return-to-one state transition.
- *Bgd* and *Bgps*: The *Bgd* and *Bgps* Time Domain SWs are nearly indistinguishable in Figure 7 at the transitions. However, the short between the input and the power supply in the *Bgps* macrocells cause a DC offset in the supply voltage during steady-state that is evident in Figures 7 and 8. When different supplies are used, as shown in Figures 9 through 12, the SWs are nearly indistinguishable at all points.

The Bridging experiment Phase SWs of Figures 7, 8 and 9 are difficult to distinguish below 250 MHz but the Magnitude SWs are sufficiently distinctive to distinguish among the different types of defects. The bridging experiments indicate that a significant amount of additional transient variation can be expected from shorting defects when compared with the variation introduced by open defects or defect-free operation.

4.0 Summary and Conclusions

We have presented results of hardware experiments designed to evaluate the effectiveness of transient signal analysis in the characterization of CMOS defects and its potential application to failure analysis. We evaluated data from test structures into which we introduced seven types of shorting and open defects. The data was collected from non-defective test structures that were coupled to defective test structures through each of four different coupling mechanisms. The analysis was carried out by comparing the time and frequency domain representation of the transient signals. We showed that it is possible to distinguish between the various defect types using these signals in one or more of the Time, Magnitude or Phase domains.

In particular, we verified that the Time Domain Coupled waveforms were consistent with the signal behavior on the output of the defective inverters. We also determined that defects which cause transistor gates to float were most easily distinguished using the Phase representation of the signals. This was also true for open drains. In contrast, open sources and bridging defects were most easily distinguished using the Magnitude representation.

We also evaluated the relative contribution of each of the coupling mechanisms to the signals measured on the coupled test pads. Our experimental structure controlled for each of four coupling mechanisms, power supply, internodal, well and substrate. We showed that the predominant coupling mechanism is the power supply but also showed that n-well coupling produced measurable variations. In addition, we determined that internodal and p-well coupling, though measurable, were much less significant than the power supply and n-well coupling mechanisms.

These result suggest that measuring the transients at multiple positions on the power supply would increase sensitivity to defects and reduce the number of test points necessary for the test to be effective. The power supply is attractive for other reasons as well. Since the power supply is globally routed, a great deal of freedom exists in the placement of the test points with respect to the underlying logic under test. Moreover, the capacitive load associated with the test point pads does not have an impact on circuit performance as is true if logic output nodes are monitored instead. We are planning additional hardware experiments to investigate this possibility.

We have already shown in our defect detection experiments in TSA that there is a regional aspect to the signal variations that result from defects. We also determined that the variations caused by process tolerance effects were global and that we could calibrate for them by cross-correlating Signature Waveforms at multiple test points. We expect that we can use the same procedure to deal with process tolerance effects here. Moreover, in the context of failure analysis, the regional nature of the variation introduced by defects in the signals of multiple test points can also be useful in generating information on the location of the defect. We are currently redesigning our test device to investigate this possibility.

We also determined that a high degree of correlation exists among the waveforms measured from identically configured test structures. This is consistent with our expectations that intra-device process tolerances are very small. We are still gathering data from the other chips but expect this property to hold for these devices as well. The additional data will also allow us to determine how the coupled signal variations caused by defects change in the presence of inter-device process tolerance effects.

References

[1] James F. Plusquellic. “Digital Integrated Circuit Testing Using Transient Signal Analysis,” Ph.D. Dissertation, Department of Computer Science, University of Pittsburgh, August, 1997.

[2] James F. Plusquellic, Donald M. Chiarulli, and Steven P. Levitan. “Digital IC device testing by transient signal analysis (TSA),” *Electronics Letters*, 31(18):1568–1570, August 1995.

[3] James F. Plusquellic, Donald M. Chiarulli, and Steven P. Levitan. “Digital Integrated Circuit Testing using Transient Signal Analysis,” *International Test Conference*, pp. 481-490, October 1996.

[4] James F. Plusquellic, Donald M. Chiarulli, and Steven P. Levitan. “Identification of Defective CMOS Devices using Correlation and Regression Analysis of Frequency Domain Transient Signal Data,” *International Test Conference*, pp. 40-49, November 1997.

[5] David P. Vallett, “An Overview of CMOS VLSI Failure Analysis and the Importance of Test and Diagnostics,” ITC Lecture Series II, Practical Aspects of IC Diagnosis and Failure Analysis: A Walk through the Process, Lecture 2.1, *International Test Conference*, October 1996.

[6] Yeoh Eng Hong and Martin Tay Tiong We, “The Application of Novel Failure Analysis Techniques for Advanced Multi-Layered CMOS Devices,” *International Test Conference*, pp. 304-309, November 1997.

[7] Christopher L. Henderson and Jerry M. Soden, “Signature Analysis for IC Diagnosis and Failure Analysis” *International Test Conference*, pp. 310-318, November 1997.

[8] Jerry M. Soden, Richard E. Anderson, and Christopher L. Henderson, “IC Failure Analysis Tools and Techniques - Magic, Mystery, and Science,” ITC Lecture Series II, Practical Aspects of IC Diagnosis and Failure Analysis: A Walk through the Process, Lecture 2.5, *International Test Conference*, October 1996.

[9] Jerry M. Soden and Charles F. Hawkins. Electrical Properties and Detection Methods for CMOS IC Defects. In *Proceeding of the European Test Conference*, pages 159–167, 1989.

[10] Charles F. Hawkins, Jerry M. Soden, A. Righter and Joel Ferguson, “Defect Classes - An Overdue Theory Paradigm for CMOS IC Testing,” *International Test Conference*, November 1994.

[11] Robert Aitken, “A Comparison of Defect Models for Fault Location with IDDQ Measurements,” *International Test Conference*, pp. 778-787, November 1992.

[12] Kenneth L. Shepard and Vinod Narayanan, “Noise in Deep Submicron Digital Design,” *International Conference on Computer-Aided Design*, pp. 524-531, November 1996.