High-Speed Optoelectronics Receivers in SiGe

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Abstract

This paper focuses on the investigation of integrated CMOS and Silicon/Germanium (SiGe) devices for high-speed optical receiver circuits. In this paper, we present several competitive designs of front-end transimpedance amplifiers (TIA) for optical receiver applications using the IBM 5HP (0.5micron) SiGe technology. This technology exhibits f_T and f_{MAX} of 47GHz and 65GHz respectively. Spectre simulations in the Cadence Affirma analog design environment are conducted for both the TIA's and a complete receiver circuit consisting of a TIA, a cascaded multi-stage differential amplifier and a multi-stage inverting amplifier at the single supply voltage of 3.3V. We also discuss the practicality of using SiGe based photodetectors for 1.3-1.5um wavelength light and the use of Neolinear's NeoCircuit/NeoCell mixed signal design tools for optimization of the analog circuits.

1. Introduction

In this paper we present the results of our investigation on the use of IBM SiGe devices in high-speed optical receiver circuits. This investigation has two goals. First, we are investigating the practicality of using SiGe HBT phototransistors and photodiodes as photodetectors for 1.3-1.5um wavelength light. These wavelengths are used by the telecommunications industry for "long haul" fiber. However, pure silicon based detectors have very low responsivity to these longer wavelengths. Second, we are investigating the performance of a variety of high-speed analog receiver circuits based on the devices available in the IBM 5HP 0.5um SiGe Process. This investigation is motivated by the availability of this process through the IBM SiGe foundry runs provided by MOSIS [1]. In this work we have used the Neolinear Inc. mixed signal design tools for optimization of both circuit sizing and layout.

The overall project flow is shown in Figure 1. We have identified and designed circuits for the receivers as well as defined device structures, in terms of layout, for the photodetectors. We used both Cadence and Neolinear design tools for circuit design and layout. In this work with Neolinear we have first, incorporated the IBM BlueLogic BiCMOS device models into the design framework with the Cadence Affirma analog design environment and second, examined the specific types of circuit structures required for high-speed optoelectronic receivers. Using these tools we have set up a number of optoelectronics receiver designs, generated the appropriate evaluation tests and goals and used NeoCircuit to optimize the circuits for various applications.

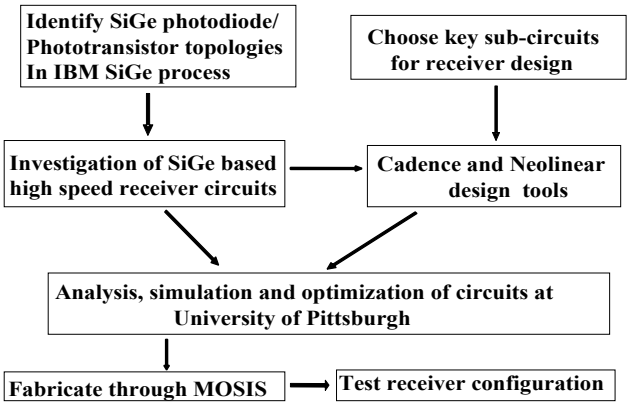

Figure 1. Project flow

2. Investigation on SiGe Photodetectors

Many researchers have looked at the possibility of using SiGe devices as high speed, low noise photodetectors in the near-IR spectrum from 850nm to1550nm. In theory, these detectors can cover the range of both free space and fiber optic communication wavelengths. Photodetection has been implemented with SiGe MSM (Metal Semiconductor Metal), PIN (P-Insulator-N), hetero-structure photo diodes and phototransistors. A second technique is the use of SiGe in MSM photodiodes. A third class of SiGe photodetectors is based on a vertical cavity multi-layer P-I-N diode. Finally,

several researchers have investigated the use of SiGe photodiodes for photo detection in 1.3µm - 1.55µm range [2-11].

3. Motivation and present work

The availability of the access to the new IBM SiGe process (Blue Logic) has prompted us to investigate the use of similar structures for this process. However, the fixed structures available in this commercial process drive us to consider a SiGe BJT phototransistor structure integrated with the available CMOS structures. IBM's Blue Logic SiGe process is a BiCMOS process, which has available two kinds of NPN HBT (SiGe bipolar) transistors as well as N and P channel MOSFETs. We examined several methods of photodetection, using this process, as well as multiple circuit configurations for amplification and thresholding. SiGe photodetectors can be made by exposing the SiGe "base" layer of the HBT structure, as shown in Figure 2

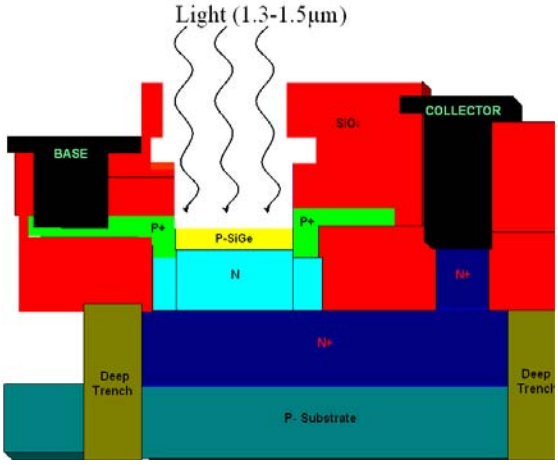

Figure 2. Cross section view of IBM SiGe NPN transistor with exposed base for phototransistor

The initial photo-detector design was based on a SiGe npn transistor layout. It was determined that several layers are responsible for forming of the SiGe base and afterwards the emitter directly above it. However, for a successful photo-detector a path is needed for light to reach SiGe base. Therefore the emitter had to be partially or fully removed. If the emitter is removed, the SiGe layer can be exposed to external light, creating a photodiode. On the other hand, if the base contact is removed and the emitter contact is maintained we create a phototransistor. Based on this idea several versions of photo-detectors were created. To the authors' knowledge, no SiGe based photodetectors in IBM 5HP technology have yet been reported.

3.0 Architecture for the optical receiver

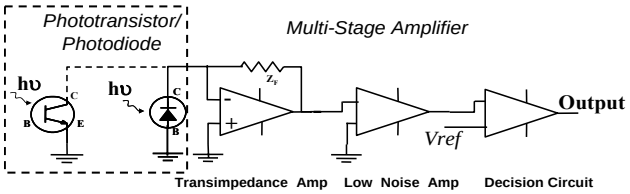

Figure 3. Key components of optical receiver circuit

As shown in Figure 3 the front-end of the receiver circuit consists of photodetector followed by a transimpedance amplifier, cascaded differential amplifers and a decision circuit. Based on this idea several TIA's have been simulated the results of which are shown in Table 1.

Table 1. Pre and post-layout simulation results of transimpedance amplifier circuits

	Pre-Simulation			Post-Simulation (RCX)		Post-Simulation (RCX with I/O Pads)					
Circuit/ Topology	Output (mV)	Bandwidth (GHz)	Feedback Resistance R_f (Ω)	Output (mV)	Bandwidth (GHz)	Output (mV)	Bandwidth (GHz)	Gain (dB Ω)	Physical Verification by DIVA DRC	EXT	LVS
TIA#1	6.56	10.11	700 (Ω)	6.55	10.18GHz	6.55	9.12GHz	56.32	✓	✓	✓
TIA#2	15.04	9.99	430 (Ω)	14.56	10.14GHz	14.56	9.86GHz	63.26	✓	✓	✓
TIA#3	19.60	9.96	700 (Ω)	19.11	9.84GHz	19.11	2.19GHz	65.62	✓	✓	✓
TIA#4	6.70	10.34	700 (Ω)	6.82	8.41GHz	6.82	8.45GHz	56.67	✓	✓	✓
TIA#5	25.52	10.93	630 (Ω)	24.41	9.54GHz	24.41	9.49GHz	67.75	✓	✓	✓
TIA#6	29.99	6.41	680 (Ω)	29.12	6.01GHz	29.12	5.21GHz	69.28	✓	✓	✓
TIA#7	46.73	3.33	680 (Ω)	47.50	2.97GHz	47.50	2.72GHz	73.53	✓	✓	✓
TIA#8	21.57	9.99	700 (Ω)	21.49	8.59GHz	21.49	1.84GHz	66.64	✓	✓	✓
TIA#9	5.70	10.06	700 (Ω)	5.77	8.33GHz	5.77	8.12GHz	55.22	✓	✓	✓
TIA#10	5.57	5.1	100 (Ω)	5.06	2.94GHz	5.06	2.97GHz	54.08	✓	✓	✓
TIA#11	10.25	10.48	700 (Ω)	10.04	7.96GHz	10.04	5.45GHz	60.03	✓	✓	✓
TIA#12	15.03	10.66	700 (Ω)	14.06	9.04GHZ	14.76	7.96GHZ	63.38	✓	✓	✓
TIA#13	31.06	11.44	580 (Ω)	28.01	7.70GHz	28.01	5.78GHz	68.94	✓	✓	✓
TIA#14	14.60	12.83	690 (Ω)	15.29	8.34GHz	15.29	4.22GHz	63.69	✓	✓	✓

TIA#1-TIA#8 are based on a similar architecture in which the front end consists of common emitter amplifier followed by a feedback resistance (Rf). This feedback is used to vary the input and output resistance of the first stage. Figure 4 shows a schematic of TIA#6 consisting of npn transistors Q1 and Q2 as a common emitter stage followed by two cascaded common emitter stages Q3 and Q4 for high gain and bandwidth. The output stage consists of npn transistor Q5 as a emitter follower which acts as a buffer.

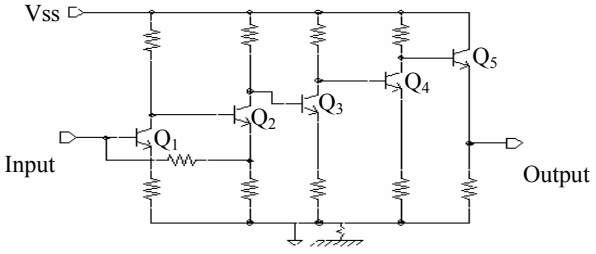

Figure 4. Circuit topology TIA#6

Figure 5 and Figure 6 show the transient and AC analysis of TIA#6 for the pre-layout and post-layout simulation at 10GHz. The post-layout simulation results include the intrinsic parasitics and the I/O pads. TIA#9-TIA#14 [12-16] are SiGe based transimpedance amplifiers based on different configurations simulated in IBM SiGe process to compare their respective performance.

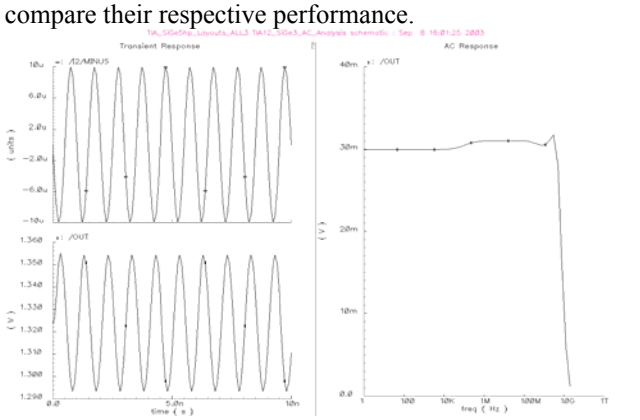

Figure 5. Pre-Simulation of TIA#6 at 10 GHz

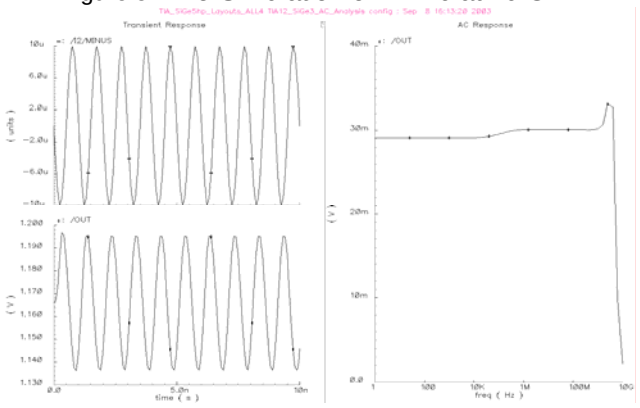

Figure 6. Post-Simulation of TIA#6 at 10 GHz

4.0 Optical receiver circuit design

Figure 7 shows the complete receiver circuit consisting of TIA#11 as the front end architecture followed by three differential amplifier stages Q1 Q2, Q3 Q4 and Q5 Q6 biased by NFET transistor N1, N2, N3 respectively. The output of the first differential stage is taken dual ended in order to achieve maximum gain. The output of the third differential amplifier is taken single ended followed by a Darlington pair buffer stage Q7 and Q8 to buffer the output without affecting the amplified voltage from the previous differential stages. The last stage is the decision circuit stage which is a CMOS inverter used to compare the output of the buffer circuit to a threshold level and determine at each bit slot whether the signal element is a binary '1' or a binary '0'. Figure 8 shows the output for all the intermediate stages for an input current of 10μamps.

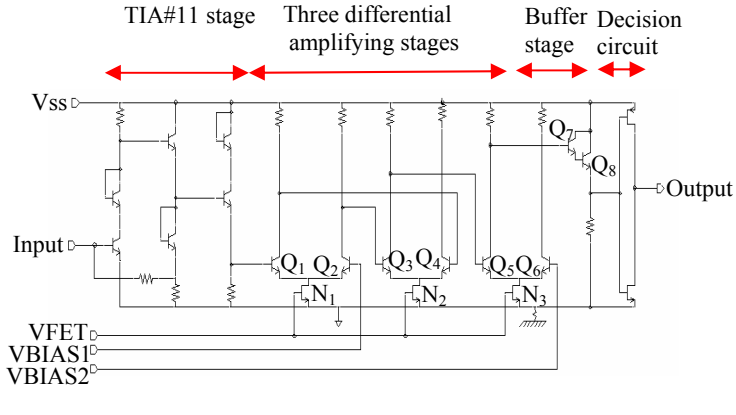

Figure 7. Complete receiver circuit at 2Gb/s

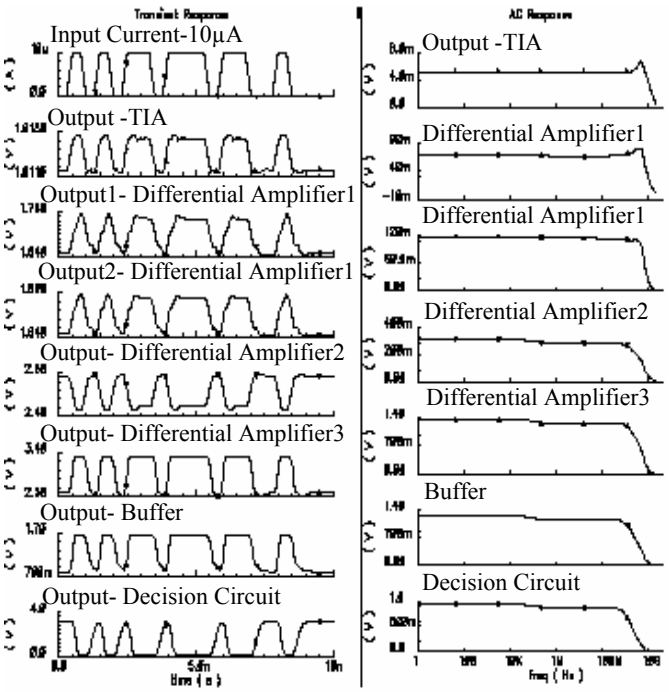

Figure 8. Output waveform of complete receiver circuit

Conclusion

An investigation on SiGe photodetectors in the IBM SiGe 5HP process has been carried out successfully and, on this basis, several arrays of SiGe photodetectors have been built on a test chip as shown in Figure 9. Sixteen transimpedance amplifiers, each simulated to work with a minimum input current of 10μA, have been designed and simulated using the Cadence Spectre simulator. Simulations, with extracted parasitic resistance and capacitance, predict that the receiver circuits will work at 2Gb/s. At the time of writing, the chip has been sent for fabrication to MOSIS.

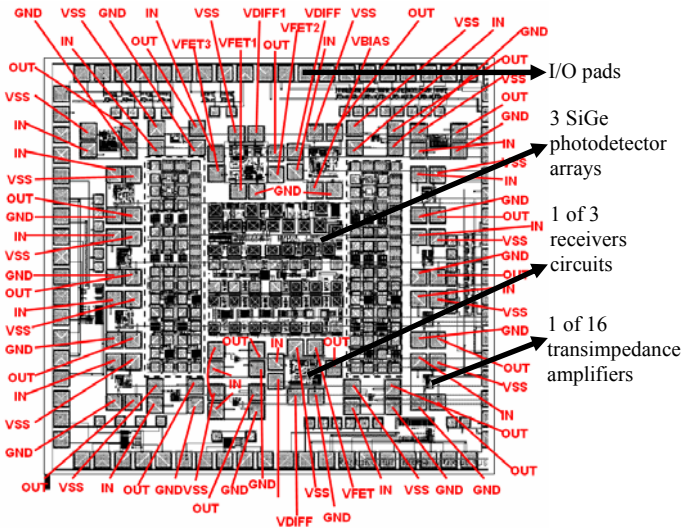

Figure 9 Test Chip Layout (3x3.3mm) showing the 16 transimpedence amplifiers, three receiver circuits and three different arrays of test structures for photodetectors

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References

[1] MOSIS Process Information IBM Microelectronics SiGe BiCMOS 5HP – 0.50 micron feature size, www.mosis.org/Technical/Process/proc-ibm-5hp.html

[2] L. Naval, et. al., "Optimization of Si1-xGex/Si waveguide photodetectors operating at λ=1.3µm", IEEE Journal of Lightwave Technology, Vol. 14, No. 5, may 1996, pp. 787-797.

[3] F. Y. Huang, et. al., "Epitaxial SiGeC/Si photodetectors with response in the 1.3µm - 1.55µm range", Electron Devices Meeting, 1996., International , 8-11 Dec. 1996, pp. 665 -668.

[4] F.Y Huang, et. al, "Normal-incidence epitaxial SiGeC photodetector near 1.3µm wavelength grown on Si substrate", Appl. Phys. Lett., Vol. 69, No. 16, 14 Oct. 1996, pp. 2330-2332.

[5] "H. Temkin, et. al.,"High photoconductive gain in GexSi1-x/Si strained-layer superlattice detectors operating at λ=1.3µm," Appl. Phys. Lett., Vol. 49, No. 3, 21 July 1986, pp. 155-157.

[6] F. Y. Huang, et. al., "Epitaxial SiGeC waveguide photodetector grown on Si substrate with response in the 1.3µm - 1.55µm wavelength range", IEEE Photonics Technology Letters, Vol. 9, No. 2, Feb. 1997, pp. 229-30.

[7] A. Splett et. al., "Integration of waveguides and photodetectors in SiGe for 1.3µm", IEEE Photonics Technology Letters, Vol. 6, No. 1, 1994, pp. 59-61.

[8] V. P. Kesan, et. al.,"Integrated waveguide-photodetectors using Si/SiGe multiple quantum wells for long wavelength applications", Electron Devices Meeting, 1990. Technical Digest, International, 9-12 Dec.1990, pp. 637-40.

[9] James Kolodzey edited by Maurice H. Francombe, "Silicon Germanium alloy devices", Chapter 6, , Handbook of thin film devices, Vol. 1: Heterostuctures for high performance devices, Published: San Diego : Academic Press, c2000.

[10] C. K. Maiti, G. A. Armstrong, "Application of Silicon-Germanium heterostructure devices", Chapter 9, SiGe Optoelectronic Devices, Published by: Institute of Physics Publishing 2001.

[11] C. K. Maiti, et. al., "Strained silicon heterostructures materials and devices", Chapter 10 Si/SiGe Optoelectronics, Published by: The institution of Electrical Engineers, 2001.

[12] Sung Min Park, et. al., "A high-speed four-channel integrated optical receiver array using SiGe HBT technology", IEEE International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland, pp. v433-6.

[13] C. B. Yahya "Design of wideband low noise transimpedance amplifiers for optical communications", Proc. 43rd IEEE Midwest Symp. On Circuits and Systems, Lansing MI, Aug 8-11, 2000, pp. 804-7.

[14] J. –S. Reih, O. Qasaimeh et. al., "Monolithically integrated SiGe/Si PIN-HBT front-end transimpedance photoreceivers", High Speed Semiconductor Devices and Circuits, Proceedings, 1997 IEEE/Cornell Conference on Advanced Concepts, 4-6 Aug. 1997, pp. 321-31.

[15] Y. Amamiya, Y. Suzuki et. al., "40-Gb/s optical receiver IC chipset – including a transimpedance amplifier, a differential amplifier, and a decision circuit – using GaAs-based HBT technology", Microwave Symposium Digest, 2002 IEEE MTT-S International, Volume 1, 2-7 June 2002, pp. 87-90.

[16] S. Lee, P. J. G. Dave et. al., "Hybrid optical receivers with integrated electronics", Optical Detectors and Receivers, IEE Colloquium, 27 Oct 1993, pp. 6/1-4