Area, Power, and Pin Efficient Bus Transceiver Using Multi-Bit-Differential Signaling

Donald M. Chiarulli
Dept of Computer Science
University of Pittsburgh
Pittsburgh, PA USA

Jason D. Bakos
Dept of Computer Science
University of Pittsburgh
Pittsburgh, PA USA

Joel R. Martin
Dept of Computer Science
University of Pittsburgh
Pittsburgh, PA USA

Steven P. Levitan
Electrical and Comp. Eng.
University of Pittsburgh
Pittsburgh, PA USA

***Abstract*—This paper describes a new low-power, area and pin efficient alternative to differential encoding for high performance chip-to-chip and backplane signaling. The technique, called multi-bit-differential-signaling (MBDS), consists of a new design for the driver and link termination network coupled with a novel coding system based on N choose M (nCm) codes. In an nCm coded MBDS channel, there are *n* physical interconnections over which all code symbols carry exactly *m* 1-bits. This property gives MBDS links signal-to-noise and transmission characteristics comparable to pair-wise differential links such as low-voltage differential signaling (LVDS). Moreover, MBDS is compatible with commercial LVDS receivers in point-to-point and multi-point bus topologies. However, because MBDS channels have a higher information density, they use up to 45% less power and up to 45% fewer I/O pads than equivalent differentially encoded buses.**

I. Introduction

There are two important trends in digital integrated circuit technology that are motivating designers to seek higher bandwidth off-chip signaling solutions. The first is a technology trend driven by the traditional gap between on-chip and off-chip signal bandwidth. This gap continues to widen as CMOS technology advances faster than PCB fabrication and materials technology and has become a substantial bottleneck in overall system performance. The second trend is based on changes in the economics of chip production for high speed and low power devices in deep sub-micron technologies. When measuring overall power consumption, silicon real estate and chip packaging costs for these devices, it is cheaper to organize the off-chip signaling into a small number of high speed I/O lines rather than the traditional bit-per-pin I/O organizations.

Consistent with this trend, Intel has projected I/O links capable of 10 Gbps over 40cm of FR-4 PCB material in near-term generations of their microprocessors [1]. For the present, commercial signaling standards have emerged in the 200 to 800Mbps per pin range. Examples include Hypertransport[2], a bus standard at 400Mbps/pin, QRSL [3] a high density memory interconnect from RAMBUS that achieves 800Mbps/pin using 4-level logic, and two serial LVDS standards, TIA/EIA-644-A at 655Mbps and IEEE 1563 at 500Mbps [4]. At gigabit rates Hypertransport 2 has emerged this year with a 1Gbps per pin speed grade option at the high end [5].

It is clear that for any standard for high-speed chip-to-chip links, channel coding will be based on some form of differential signaling [6]. In a differential channel, each bit is encoded based on an oppositely charged pair of transmission lines. Each state, zero or one, is encoded as one of two code words represented by the two polarities, on-off or off-on. Differential signaling has significant advantages for managing losses and signal-to-noise ratio in high-speed communication links. The disadvantage of differential signaling is that it suffers from very low code density, using only half of the signaling capacity of two single-ended transmission lines.

We have devised an alternative to differential signaling for high-speed link applications. The new method, called Multi-Bit-Differential Signaling (MBDS), retains the noise and loss advantages of a differential channel, but significantly increases the code density of differentially encoded bus structures. By exploiting a larger set of assignable code symbols, an MBDS encoded bus can send the same information using fewer physical connections than an equivalent differentially encoded bus. The result is a substantial savings in power, area, and pad count.

II. Multi-Bit Differential Signaling

There are three novel concepts that together enable MBDS links. All are embodied in Figure 1. The first is a new driver based on a current-steering design extended to drive

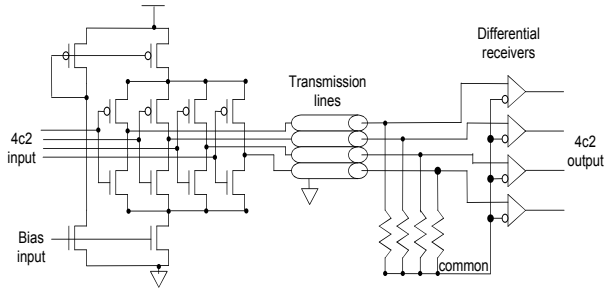

Figure 1. Example MBDS Link

multiple current mode logic channels. The second is a novel termination network that terminates each channel to a single point and creates a self consistent common node within the network, and the third is an "*n* choose *m*" (written nCm) encoding rule for the data symbols in the channel such that each *n*-bit symbol encoding must have exactly *m* 1-bits and (*n*-*m*) 0-bits.

Like other high-speed serial links, an MBDS link uses current mode logic in which the driver circuit, shown on the left side of Figure 1, operates by steering a constant supply current through different paths in the termination network. All of the resistors in the termination network have the same value, chosen to match the impedance of the transmission lines, regardless of the width of the link. Each resistor is wired between its corresponding transmission line and common node shared by all of the termination resistors. Since every MBDS code symbol is encoded with exactly the same number of 1-bits and the current-per-bit (I_{bit}) is constant, the voltage of the common node is constant.

Data is encoded by the direction of current flow through the termination network with one bit through each termination resistor. For example in the 4C2 example of Figure 1, exactly two of the termination resistors will each source I_{bit} into the common node. Exactly two others will always sink the same current. A differential receiver between the transmission line output and the common node reference senses each data bit as a differential voltage that changes polarity in each state relative to the common node voltage.

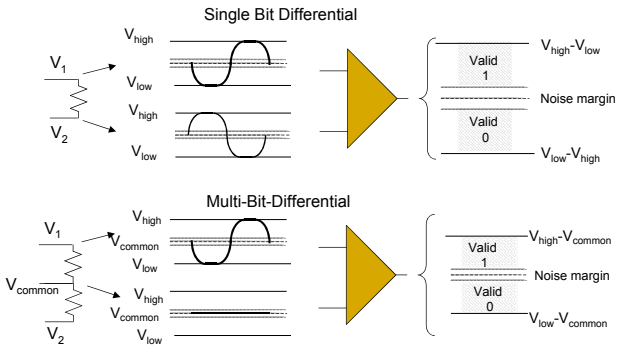

Figure 2. Comparision of single-bit and multi-bit differential signals showing scaling effects of signal voltage and signal to noise margin.

Unlike a conventional differential transceiver where signal and noise appears on both legs of the differential receiver, an MBDS receiver sees signal and common mode noise on one leg, and only the common mode noise on the other. This configuration is shown in Figure 2. It has equivalent common mode noise rejection but a smaller differential signal voltage. However, even with a smaller signal voltage, signal to noise ratio and noise margin are comparable. This is because the termination network divides both the data signal and noise powers equally and references the difference to the center voltage of the common node.

A more significant issue is the performance of MBDS channels as they are scaled to larger bit widths. In this respect MBDS has very favorable architecture. All of the major components in the link scale independently. Specifically, the receiver amplifiers are pair-wise differential with constant circuit complexity under scaling. The number of legs in the driver circuit and number of resistors in the termination network grows linearly in the number of wires in the link. However, the size of the termination resistors is constant under scaling as is the signal voltage assuming that the current-per-bit is constant. The only components of the transceiver circuitry that grows with channel width are the biasing transistors in the driver. The total bias current increases with the channel width in multiples of the number of 1-bits in the encoding. Given that the typical current-per-bit value is three to five milliamps, this is not a significant issue and even as a potential source of noise it will be common mode and thus rejected.

III. N CHOOSE M (NCM) ENCODING

The code density advantages of MBDS links arise from the nCm encoding rules for code symbols. In any particular channel configuration these advantages are expressed as a combination of lower pad count, lower power, and additional code capacity. Consider the set X such that $X_{nm} = \{x_{nm} : x \in nCm\}$. In other words, X_{nm} is the set of all valid code symbol encodings in an nCm channel. The size of X_{nm}, which is the number of available code symbols, is:

$$\phi\{X_{\mathrm{nm}}\} = \frac{\mathrm{n!}}{(\mathrm{n-m})!\,\mathrm{m!}}$$

The number of nCm code symbols is maximal when m is equal to $n/2$, rounded if the value of n is odd.

Each code symbol must be mapped to a binary data value at the inputs and outputs of the system. Since incoming and outgoing data will always be an integral number of binary bits, the effective bit width, bit_{eff}, the number of bits coming into and out of the channel before encoding and after decoding is given by:

$$bit_{eff} = \mathrm{floor}(\log_2(\phi\{X_{mn}\}))$$

Using effective bit width as a metric, Table 2 compares the relative power consumption, pad count, and code utilization for several MBDS channel configurations to a differentially encoded bus with an equivalent effective bit width. The relative power consumption is computed as $P_{eff} = m/bit_{eff}$, the ratio of m, the number of wires energized to '1' in the nCm coded channel, to bit_{eff}, the number of differentially encoded bits required to send the same information. The relative pin count is computed as $RP=n/(2*bit_{eff})$, the ratio of n, the number of wires in the nCm coded channel, to $2*bit_{eff}$, the number of differential channels required to send the same information times two wires per channel. From the data in the table it is clear that a 30-45% improvement in power efficiency and pad utilization can be achieved with relatively small values of n.

The rightmost column in the table is a measure of the number code symbols left over after encoding all of the input data words to symbols in the nCm encoding. These unused code words are available for error checking, protocol support or other link management functions. The number of excess codes varies significantly between different channel sizes. The utility of the excess codes can be greatly enhanced by combining multiple code words in temporal or spatial sequences. In a current project we are implementing complex ECC coding into MBDS buses with little or no additional code bits and no additional channel requirements other than an nCm word sequence.

TABLE I. COMPARISON OF MBDS CHANNELS TO EQUIVALENT DIFFERENTIALLY ENCODED BUSSES

Chan type	$\phi\{X_{mn}\}$	bit_{eff}	P_{eff}	RP	Code Util
2C1	2	1	100%	100%	100%
4C2	6	2	100%	100%	66%
6C3	20	4	75%	75%	80%
8C4	70	6	66%	66%	91%
10C5	252	7	71%	71%	51%
12C6	924	9	66%	66%	55%
16C8	12870	13	62%	62%	64%
32C16	601080390	29	55%	55%	89%

IV. PERFORMANCE DATA

In this section we present both simulation data and direct measurements from a test link based on the design shown in Figure 1 and with annotated circuit models shown in Figure 5. The link simulations were done in Cadence Spectre and are fully modeled including layout-extracted circuit models, package parasitics, and coupled transmission line models for an 8" link in FR4 PCB material. The transistor models used in this simulation are the *MOSFET* models from the IBM 5HP .5um SiGe process. Bandwidth performance for the test data is modest when compared to more aggressive CMOS fabrication technologies but is actually quite impressive given the capabilities of .5um SiGe MOS devices.

The eye diagrams shown in Figure 3 are from a simulation study designed to compare the performance of MBDS links under scaling. The eye diagrams shown are for 1Gbps data sensed between T0 and common of of a 2C1 (standard differential), 4C2 and 8C4 link. A circuit model of the 2c1 and 4c2 circuits is shown in Figure 5.

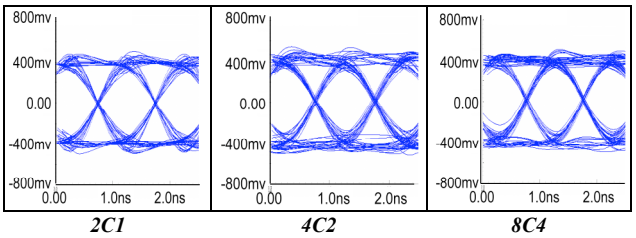

Figure 3. Comparative eye diagrams from simulations of 2C1, 4C2, and 8C4 MBDS links

From these eye diagrams there appears to be little impact on performance as we scale the system from 2C1 to 8C4. The only difference between these runs is that the bias current was increased in the larger drivers such that the total current per 1-bit was kept constant. This is very encouraging particularly since the size of the resistors in the termination network and the rail-to-rail voltage swing across the network are independent of the width of the link. Therefore, with the current-per-bit held constant by the biasing network there is no increase in the signal-to-noise ratio at each receiver input as a consequence to scaling the system.

Figure 4 shows measured data from two test links using test chips fabricated in .5um IBM 5HP SiGe technology. The left plot in Figure 4 is one channel from a 4C2 link running at 500Mbps through 8" of FR4 PCB material and measured at the output of a custom receiver circuit on a second copy of the test chip. The right plot in Figure 4 is measured data for a second test link using a commercial LVDS receiver chip (National DS90LV048A) running at 200Mbps. It should be noted that the test device is in a .5um technology and the bandwidth of the simulation and test data is limited to the switching bandwidth of this technology. The commercial LVDS receiver has similar bandwidth limitations.

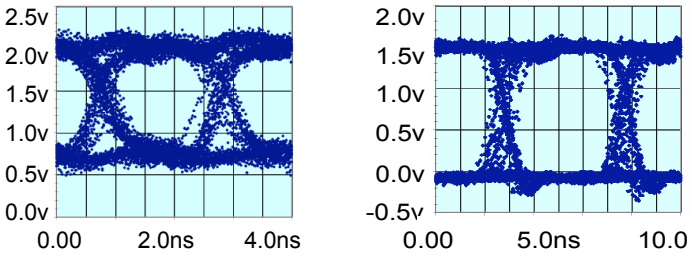

Figure 4. 500Mbs eye diagram: test link with custom receiver (left), 200Mbps eye diagram: test link with commercial LVDS receiver (right).

V. COMMON MODE NOISE ANALYSIS

In this section we present additional simulation results illustrating the common mode noise performance of MBDS links. In these simulations, a 4c2 MBDS link architecture is simulated under the same conditions as described in section IV and based on the annotated circuit models shown in Figure 5.

We performed two simulations in order to characterize common mode noise rejection in an MBDS channel. In both simulations, a common mode white Gaussian noise signal (example shown in Figure 6) was added to a valid 4C2 code word. In the first simulation, a 50mv common mode noise is injected on the $BIAS_{driver}$ input and the output signal, shown in figure 7 is measured between V_{T0} and V_{COMMON}. In the second simulation, a 200mVcommon mode noise is directly injected using separate coherent sources at nodes D1, D2, D3, and D4. The output signal at measured at the termination network, shown in figure 7, between V_{T0} and V_{COMMON} .

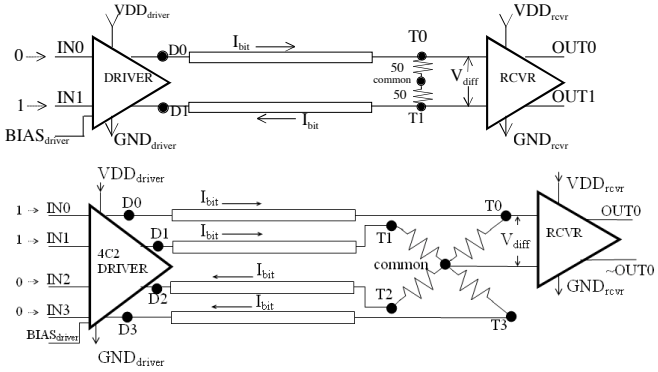

Figure 5. Electrical model of 2C1 link (top) and 4C2 link (bottom)

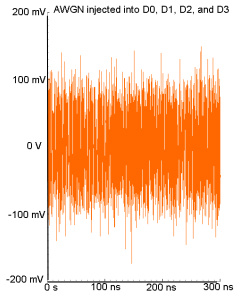

Figure 6. Additive white Gaussion noise (AWGN) signal used in common mode noise rejection simuations.

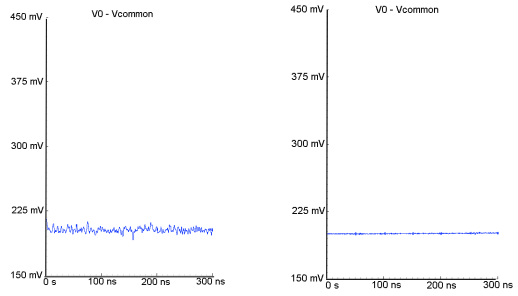

Figure 7. Simulation data for common mode noise rejection. Output signal measured between nodes V_{T0} and V_{COMMON} in Figure 5 for (LEFT) 50mV AWGN added to bias input, and (RIGHT) using four 200mV coherent sources at nodes D1, D2, D3, and D4.

VI. Noise Margins and Signal-to-Noise Ratio Simulations

To demonstrate noise margins and signal to noise relationships, we performed simulations of both a single-bit differential and an MBDS link with a single-ended noise signal added to node D0. To interpret these results, keep in mind the relationships between the termination network signal waveforms shown in Figure 2. Our purpose here is to demonstrate that in an MBDS link the total power dissipated across the termination network is the proportional for both single-bit and multi-bit differential links, assuming constant current-per-bit. However, as shown in the figure, MBDS links sense each signal relative to a common point at a medial voltage. Thus, both signal power and noise power are scaled proportionately in the output signal.

To make the measurement of relative noise versus signal power more apparent, in both simulations a pseudorandom sequence of valid encodings was transmitted with a single frequency noise source added in single-ended mode to data signal at node D0 (see figure 5). For both the single bit and MBDS simulations, I_{bit} was held constant and the same noise power (current) was injected into both tests. The results of these simulations are shown in Figure 8. Notice that in the 4c2 simulation, half of the noise power is dissipated across the T0 termination resister and the remaining power is distributed among the other bits and dissipated there in proportion to the number of bits in the code word.

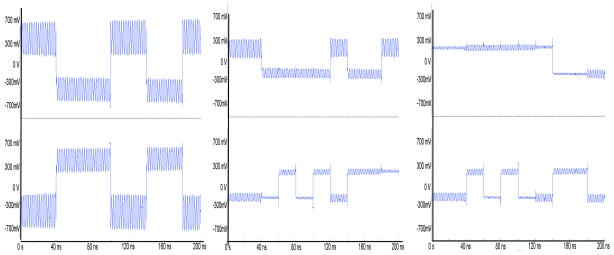

Figure 8. Signal to noise ratio demonstrations: The leftmost plot shows LVDS signals at the termination resistor. These signals are measured relative to the opposing side of the termination resistor. The rightmost two plots show MBDS signals at the termination network. Each signal is measured relative to the common node.

VII. Conclusion

In this paper we have described Multi-Bit Differential Signaling (MBDS) and the key concepts that enable it. We have shown that MBDS has a higher code density than differential signaling and retains equivalent transmission characteristics. We believe this technology meets the needs for next generation off-chip and backplane signaling.

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