Using analog memory with coupled oscillators for pattern recognition applications*

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The power/performance limitations of end-of-life CMOS are encouraging researchers to investigate new technologies for computation [Bou08]. However, to date, investigators have had little success in identifying technologies that can compete with CMOS using charge based Boolean logic [Hut08]. This leads us to rethink the use of both charge-based state and Boolean logic for the application of emerging nano-technologies.

In this work we explore the use of coupled oscillators, rather than Boolean logic, which provides for implementations using emerging nano-technology such as magnetic spin torque oscillators [Rip05] and resonant body transistor oscillators [Wein10] that have the potential of lower energy and higher density than CMOS for particular kinds of computations.

Using coupled oscillators to perform pattern matching was introduced by Hoppensteadt and Izhikevich and shown to be able to form attractor basins at the minima of a Lyapunov energy function [Hop99]. For a cluster of loosely coupled non-linear oscillators, we can use their relative phase and/or frequency relationships as a representation of state. Using this basis of state, our primitive computational operations are based on direct interactions between the frequency and phase relationships of clusters of oscillators.

For associative memory comparison operations, synchronization of the oscillators based on the degree of similarity between stored and input vectors, encoded in frequency and phase, becomes our primitive operation [Lev12]. Based on this concept, we are developing information processing systems to perform image recognition tasks by performing fast pattern recognition in high-dimension feature spaces.

Figures 1 and 2 illustrate the behavior of weakly coupled oscillators to perform matching operations. Here, we show the behavior of three coupled oscillators following the Oregonator model after [Asa05] where the model is a non-linear relaxation oscillator. In each example the oscillators' control input is a vector of analog values representing points in a vector space. In this example the "template vector" is (0.1, 0.1, 0.1) and the input is (0.1, 0.1, 0.1) for a match, or (0.19, 0.009, 0.16) which leads to a "mis-match". In Figure 1(a) we can see, soon after the start of simulation, the three oscillators converge; 1(b) shows a resistive summation of the three outputs; 1(c) shows that the integration of the summed value quickly rises to a stable value; and 1(d) shows the three oscillators output plotted parametrically to be in phase. Figure 2(a-d) shows the same data for the case that the input 3-vector is not a good match to the stored values.

Figure 3 shows an abstract view of a generic associative memory. Here, a set of associative storage words (or clusters) constitute a single large memory. The set of patterns to be matched are first stored in the memory as templates. Depending on the application, codes that correspond to the templates are also stored. Matching operations proceed by broadcasting (on a bus) input vectors to all words in the memory. Then each word performs a local comparison or match operation. This local match

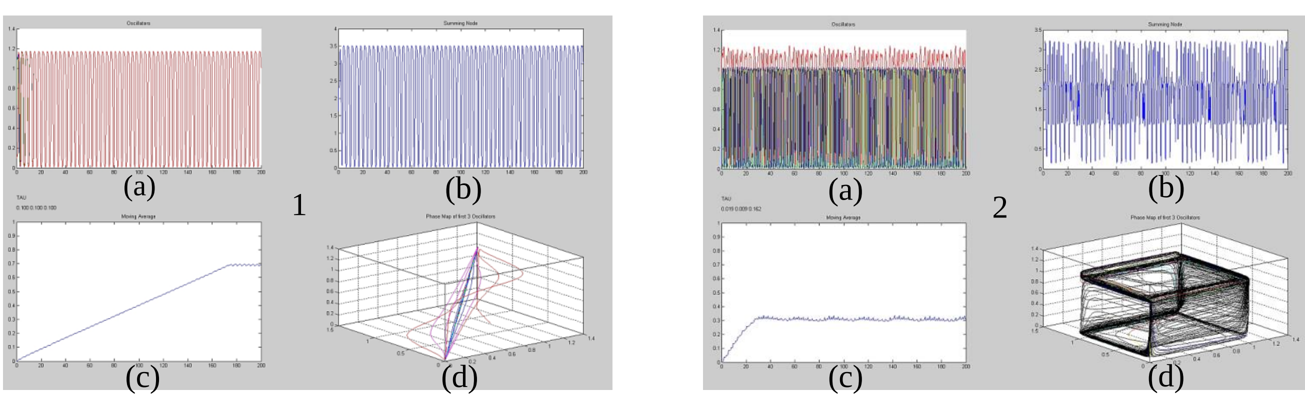
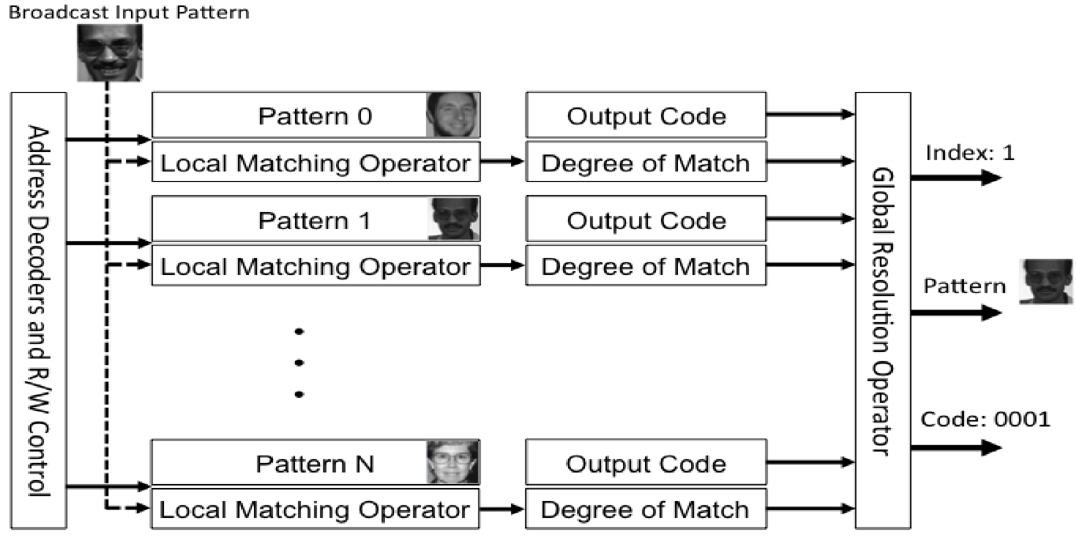


Figure 1 (Matching) and Figure 2 (Mis-Matching) behavior of three coupled oscillators. (a) Oscillator outputs; (b) summing node; (c) voltage at clipped and integrated "degree of match" node; (d) phase map of the three oscillators



Associative Memory Model for Facial Recognition

operation is relative, generating a "degree of match" between the input vector and the local template stored in the cluster (or word). Next, the degree of match from each cluster is compared and the best result is returned. Matching results can be auto-associative (returning the template), hetero-associative (returning a value from a key), or simply the index of the matching template can be returned.

Key to the operation of the memory is the calculation of the degree of match. Boolean content addressable memories typically perform an exact match or return the Hamming distance between binary vectors. On the other hand, for numeric comparisons additional circuitry needs to be added to every word of the memory such that it can locally compute a measure of the distance between the stored and input vectors. For example, for Euclidian distance between two position vectors, each word would have to compute the square-root of the sum of the squares of the pairwise differences between the coordinate values. If this is not done by each word, then the word parallelism of the associative memory is lost, and with it the primary advantage of the memory over normal sequential processing.

On the other hand, the oscillator based associative memories have two fundamental advantages over CMOS based associative processors. The oscillators have both the ability to couple based on the similarity of the input to stored vectors, and the ability of simple analog circuits to develop a degree of match without recourse to local arithmetic circuits.

However, returning to Figure 3, we see that no matter how the matching operator works, an associative memory is first and foremost a memory. And, to take full advantage of the capabilities of the analog pattern matching performed by the oscillators we need an analog memory.

Our preliminary investigations have shown that we need at least 16 and perhaps 256 levels of "gray scale" to perform pattern matching on natural scenes. This would entail the use of multiple bits of digital storage for each pixel as well as a large number of D/A converters to convert the stored template into analog values for comparison. In fact, the overhead of a large number (ideally one per pixel per word of storage) of high speed D/A converters could overshadow all the advantages of the oscillator based design.

Non-volatile, low-power, analog memory, using memristor, phase-change, or STT technology would be a perfect solution to this dilemma [Li12]. The key challenge would be in integrating those technologies with the base technology of the oscillators themselves to maintain the power, speed and area advantages of these oscillator based architectures.

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