

Design and Fabrication of SiGe Photo-Detectors in the IBM 5HP Process

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Abstract

We describe the design and fabrication of a set of integrated photo-detectors for 1.3 μ m wavelengths in the IBM 5HP commercial CMOS compatible process. Both photo-transistors and photo-diodes based on SiGe HBT NPN transistor structures were designed and fabricated.

Introduction

The goal of this project is to investigate the possibility of using a commercially available SiGe BiCMOS process to fabricate an integrated photo-detector for long haul optical networks. In the past, integrated photo-detection was incompatible with CMOS processes due to the inefficiency of silicon absorption at wavelengths above 1 μ m. The absorption spectrum of Ge and SiGe hetero structures opens the possibility of photo-detectors at longer wavelengths. In the past, SiGe photo-detectors have been fabricated with acceptable responses (in both speed and efficiency) in the laboratory [1, 2]. In this work we used the IBM blue logic 5HP commercial process for integrating such a photo-detector into CMOS VLSI circuits. The key issue we had to address was making the photo detector using legal structures.

The initial photo-detector design was based on a SiGe NPN transistor layout. It was determined that several layers are responsible for forming of the SiGe base and the emitter directly above it. However, a successful photo-detector requires a path for light to reach SiGe base. Therefore, the emitter had to be partially or fully removed. According to the SiGe process description two masks are used in building the emitter [3, 4]. The first creates the base/emitter mandrel, which is later removed to create access hole for the base in the oxide/nitride/oxide insulation layer. Afterwards a second mask builds the emitter poly above the base.

Several versions of photo-detectors were created. They were divided into photo-diodes, with the emitter completely removed, and photo-transistors, with a partial emitter contact. Both groups were further divided into three subgroups as shown in Figure 1. Version V1 had both masks present, thus providing the most complete transistor design, however significantly obstructing the path of light to the base. V2 had the first mask partially removed, thus providing better path for light, while reducing the emitter. The third version had both masks removed, thus completely exposing the base. However, the last version may affect the integrity of the SiGe base during the manufacturing process.

To further facilitate access of light to the photo-detectors another mask was added over the openings of the photo-detectors in order to prevent the formation of silicide in the path of light. Also, a topmost via was placed to create a hole in the polyimide above the detector. However, the light still needs to travel through passivation layers of the device to reach the SiGe base. Unfortunately there were no masks to create a hole or stacked hollow vias all the way to the SiGe base. Instead, it was proposed to post-process the chip die by etching holes above the photo-detectors. One feature to facilitate such etching is a ring of last metal, which may serve as a hard mask for etching solution. Rings of other metal layers for wave guiding effects may improve the detector performance. The chip (Figure 2) was designed and manufactured, and is currently undergoing testing.

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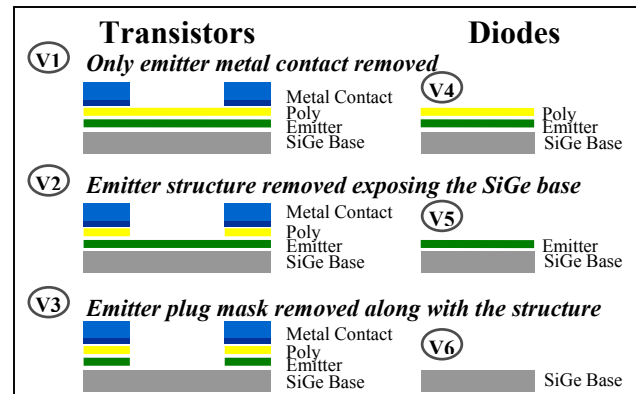


Figure 1: Photo detector cross-section views

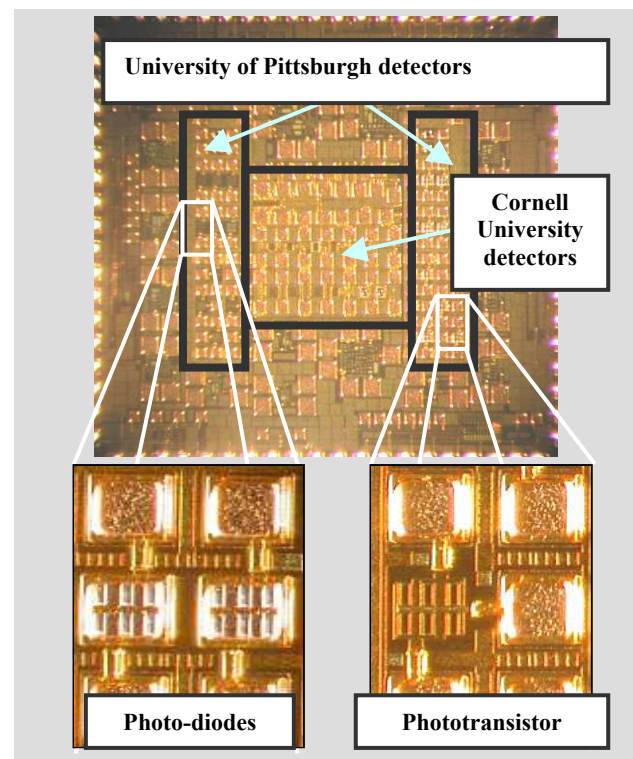


Figure 2: SiGe photo receiver chip