Piecewise Linear Large Signal Models for Optoelectronic Devices

J. A. Martinez, S. P. Levitan, D. M. Chiarulli
Departments of Electrical Engineering and Computer Science, University of Pittsburgh, Pittsburgh, PA, 15260
Jmarti@pitt.edu, steve@ee.pitt.edu, don@cs.pitt.edu

Introduction:

We have developed piecewise linear models to provide accurate (waveform) simulations of large signal (rail-to-rail) behavior of CMOS circuits, used in logic gates, the driver electronics [1] and in the transimpedance amplifiers of optoelectronic systems [2].

These models have successfully been implemented in Chatoyant [3]; a design framework and simulation tool that uses system-level models of optoelectronic (O/E) components. It provides system-level simulation and analysis for O/E devices using a Gaussian propagation based - high-level optical system simulator. Chatoyant is built on Ptolemy, a simulator framework developed at the University of California at Berkley.

Piecewise Large Signal Model for CMOS:

Many of the drivers in O/E circuits are created using complementary metal-oxide semiconductor (CMOS) inverters. They offer a simple interface between digital MOS technology in the processing section and the power hungry section of optical modulators (MQW) or sources (VSCEL). In general, models for complex MOS circuits will be non-linear functions. The computation time to solve the operation of the module using traditional node analysis and LU matrices operation is excessive for our environment [4]. Discretizing the problem makes the function linear in every time step, where we set the time step to be the sample size of the process.

Considering the classical model equations developed by Shockley [5] as characterizing the behavior of every device, a linearization of I_{ds} was performed using:

$$1)\Delta I_{ds} = g_m(P)\Delta \upsilon_{gs} + g_{ds}(P)\Delta \upsilon_{ds}$$

Where P represents any point of operation for the device. Transconductance (g_m) and conductance (g_{ds}) are the parameters characterizing the device.

Using 1) to characterize a basic driving module while considering an additive effect for the parasitic capacitances and the proper combination of linear parameters in the MOS transistors bring the representation of the piecewise linear approximation to the one shown in figure 1. g_m and g_{ds} represent the effective transconductance and conductance in the amplifier, I_{dsnet} represents the net difference between the drain currents in both transistors.

Using two-point integration to solve the difference equation and the piecewise linear approximation 1) the V-I expression for the integrated CMOS inverter is:

$$2)\ V_{ds}(t+\Delta t) = V_{ds}(t) + \frac{I_{dsnet}(t)\Delta t}{C - \frac{g_{ds}(t)\Delta t}{2}} + \left[\frac{C_{gd} + \frac{g_m(t)\Delta t}{2}}{C - \frac{g_{ds}(t)\Delta t}{2}}\right]\left[V_{gs}(t+\Delta t) - V_{gs}(t)\right]$$

This expression is the basis for our piecewise linear integration (PWLI) model for a CMOS driver.

To reduce the degree of cumulative error in the previous expression a second, exponential solution for the characteristic differential equation in the inverter was obtained:

$$3)\quad V_{ds}(t_0+\Delta t)=V_{ds}(t_0)+\frac{I_{dsnet}(t_0)}{g_{ds}}\left(e^{\frac{g_{ds}\Delta t}{C}}-1\right)+\frac{g_m}{g_{ds}}\left[\frac{\left(\frac{C_{gd}}{g_m}+\frac{C}{g_{ds}}\right)}{\Delta t}\left(e^{\frac{g_{ds}\Delta t}{C}}-1\right)-1\right]\left(V_{gs}(t_0+\Delta t)-V_{gs}(t_0)\right)$$

This expression is the basis for our piecewise linear exponential (PWLE) model for a CMOS driver.

Understanding that the degree of accuracy of the models depends mainly on the step size chosen for the time base, an *adaptive control method* for the time steps was added to the models. A binary search over the time step interval is the basis for this dynamic algorithm.

Experiments:

To show the speed and accuracy of our models, we performed several experiments comparing our results to that of Spice 3f4 (Level II).

The first test was the dynamic performance of a single CMOS amplifier under large signal input. Figure 2 shows the response of Spice vs. a simulation using the exponential model (PWLE) under a sinusoid input with f =100MHz. As can be seen, the curves are almost on top of each other. The percentage of error is well below 4 % in the middle range frequencies (100 MHz).

For our second test, we show our ability to capture the feed-forward effects within the models. Figure 3 shows us how increasing the operating frequency to 600 MHz will bring the expected overshoot from the inverter as an effect of the high frequency path created through the parasitic effective capacitance.

The third test was a multistage experiment using Chatoyant as the framework with a significant number of drivers. PWL models with a fixed sampling rate and PWL models with an adaptive sampling rate (PWLA) were tested vs. Spice at 10, 100, 500 and 1000 MHz. Figure 3 shows that the speed up achieved for the same number of timepoints is at least two orders of magnitude faster than Spice. It also shows that the adaptive algorithm for time step control (PWLA) effectively reduces the execution time compared to PWL models alone. The adaptive algorithm also improves the stability of the model. PWLA is able to give solutions to the system even where the PWL fails. This test also shows the autonomous operation of PWLA and PWL. The efficiency of both models in this range is independent of the frequency.

A complete Optoelectronic simulation of a 4f optical communication link is presented in figure 4. The input to the system is a signal of 300 Mbs. A Gaussian noise with variance of 1 V has been added to the multistage driver system to show the ability of PWL Models to respond to arbitrary waveforms. In the figure several snapshots show the behavior of the CMOS drivers under a noisy signal. Noise with levels over the threshold caused an effective change in state in the inverter. Interesting effects to note are the difference in amplifications in the noise depending on the output level, the immunity to noise and recovery of the signal offered by the inverter CMOS sections, and the cut off of negative noise spikes in the source because of the VCSEL threshold.

Discussion:

The models are well suited to perform accurate and fast (two orders of magnitude faster than spice, and less than 10% absolute error) simulations for the typical multistage CMOS drivers and transimpedance amplifiers widely used in optoelectronics applications. The models show good performance over the complete operating range (DC-1GHz) for large signal swings. They account for parasitic effect such as overshooting, phase shifting, bandwidth reduction, and noise response. The ability of these models to respond to arbitrary waveforms allows us to perform system level modeling including cross-talk, noise and bit error rate calculations in a discrete event simulation framework.

References:

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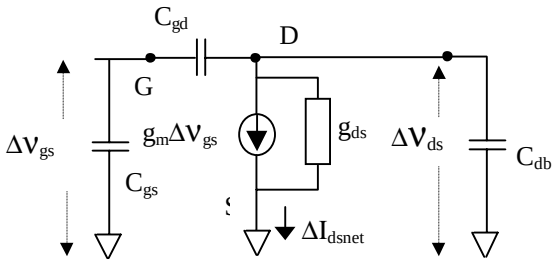

$g_m = g_{mn} - g_{mp}$; $g_{ds} = g_{dsn} + g_{dsp}$; $\Delta I_{dsnet} = \Delta I_{dsn} - \Delta I_{dsp}$

Figure 1, piecewise lineal model for the CMOS Inverter

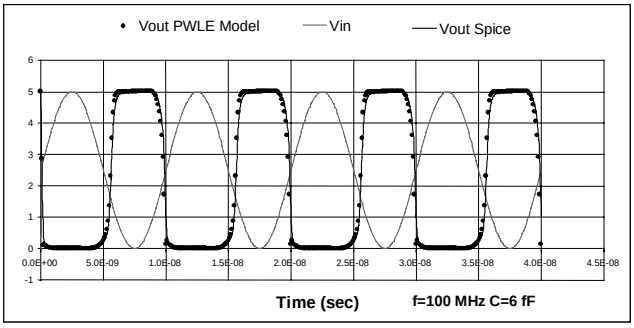

Fig. 2. PWLE and Spice output graphics under capacitive load and frequency of 100 MHz

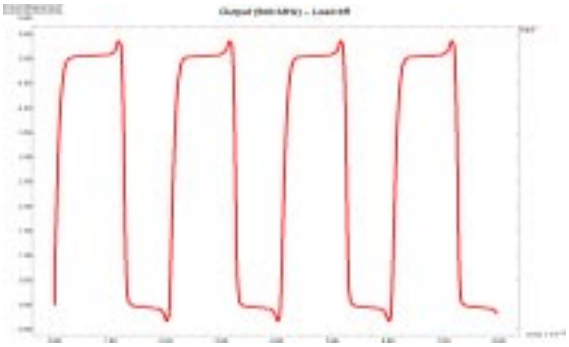

Fig. 3 Output from inverter (PWLI Model). Sinusoid input at 600 MHz, 6ff Load.

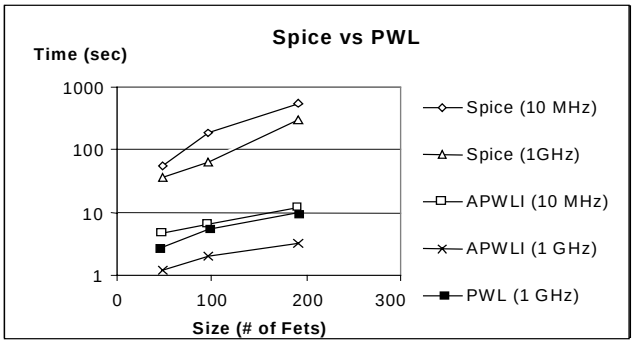

Fig. 4, Spice vs. PWL Models and APWL Models in a system of multiple FETs (f=100/500/1000 MHz).

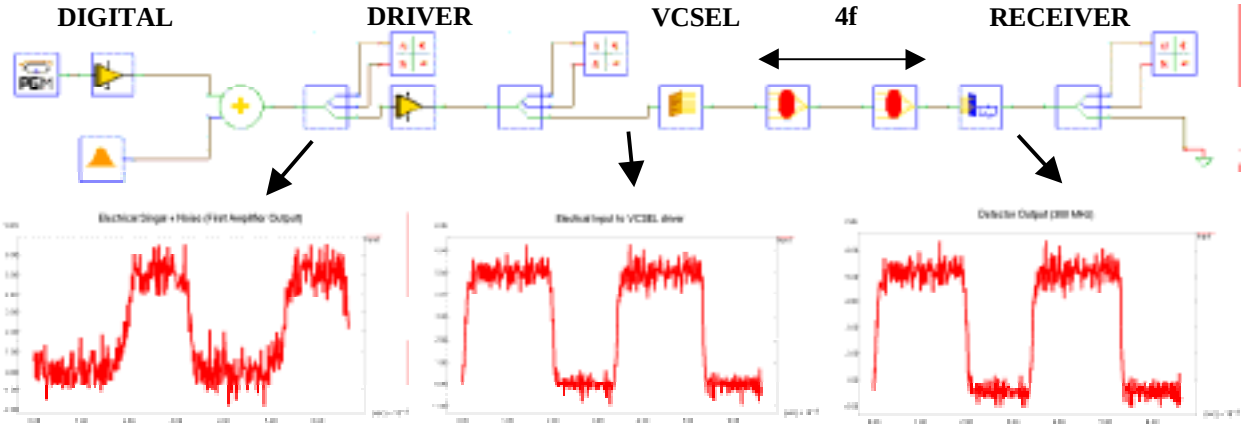

Fig. 5, Chatoyant's screen shot showing a 4f OE link system including PWL drivers and detector.