Piecewise Linear Large Signal Models for Optoelectronic Devices

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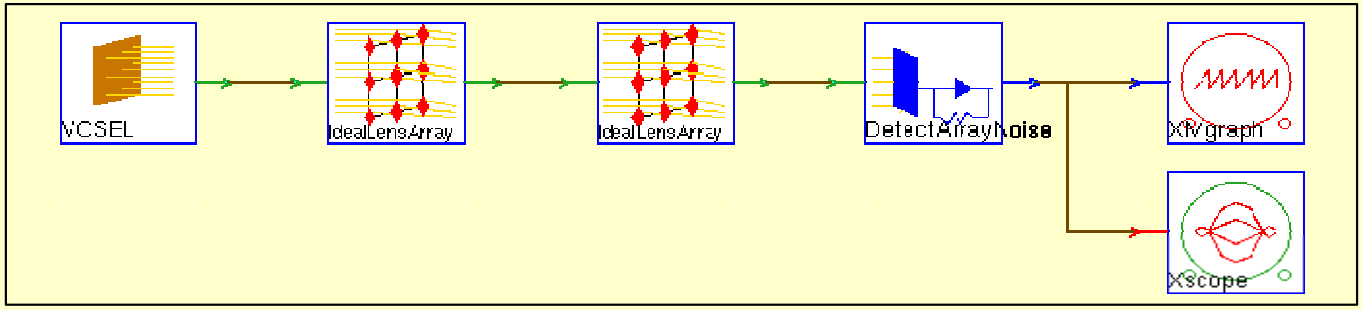
Motivation

- In a optoelectronic simulator is necessary to model the dynamics of optical, electronic and O/E interface components and their interactions.
- In this high-speed mixed technology environment we are concerned with accurate modeling of waveforms including: rise-times, delays, over-shoot, crosstalk, and noise.
- To perform system evaluation we need to effectively model both functional behavior and analog waveforms.
- Simulation of the electronic sections of optoelectronic modules should be performed in the optoelectronic simulator itself to allow design optimizations across technologies.

Goal

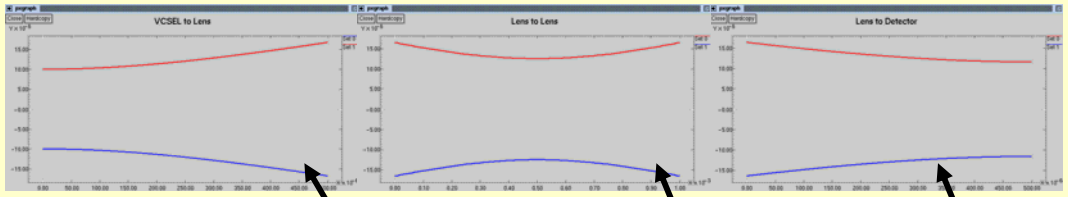
To provide accurate (waveform) simulations of large signal (rail-to-rail) behavior of CMOS circuits, used both in logic gates and in the driver electronics of optoelectronic systems, within a discrete event framework.

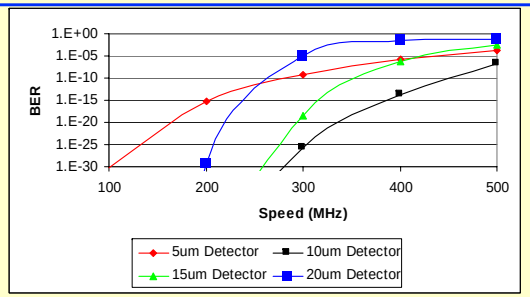
Our Optoelectronic Simulator: Chatoyant

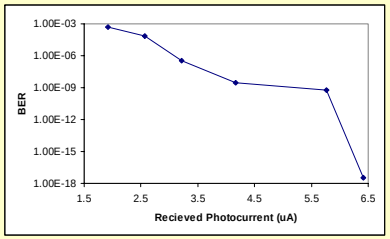


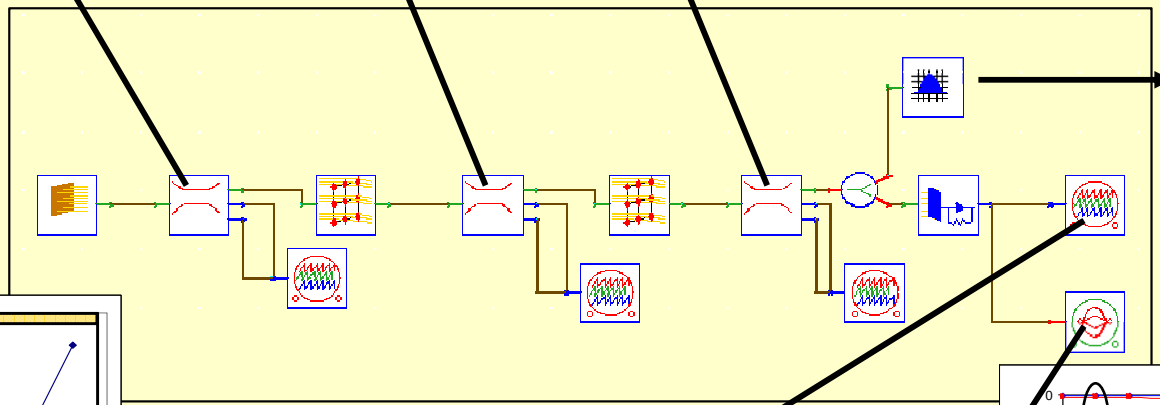
- Mixed Signal, Free-Space, Opto-Electronic Simulation Framework [See OThA2, Thursday 8:45 am]
- Built on Ptolemy (UC Berkeley)
  - Icons, called “stars”, are the component models.
    - Analytic, empirical, and “lumped parameter” models
  - Lines, or “wires”, are the signal paths.
    - Passes “message” class
    - Supports electrical and optical signal & concept of time

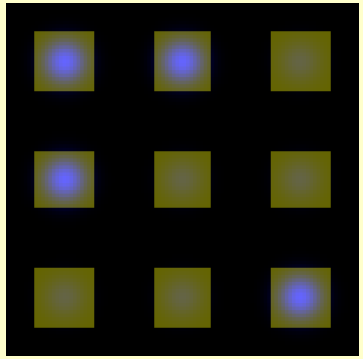
Chatoyant : Simulations and Analyses

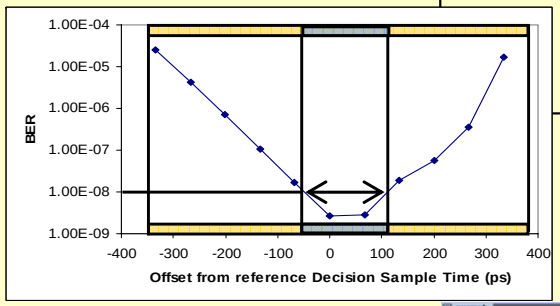


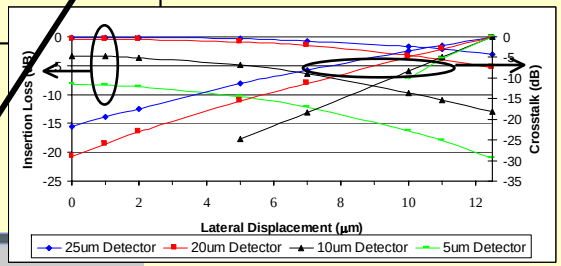


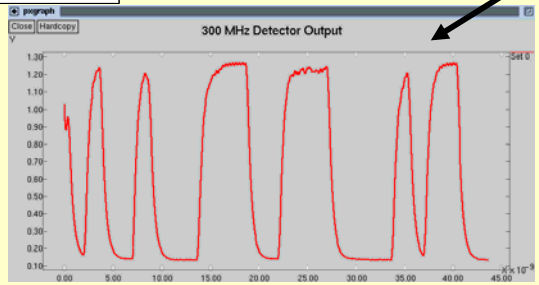


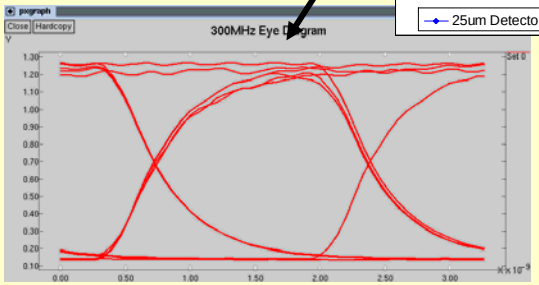












Ptolemy Constraints

- In Ptolemy systems are represented as groups of modules.
- Every module represents a model for the object, either analytical or behavioral.
- The information exchange is point-to-point between the blocks using “particles”.
- Performs dynamic simulation in a discrete time framework

Method

- Optoelectronic Device Characterization of a optoelectronic circuit would in general consist of a small to medium number of nodes:
  - A group of lumped passive devices (R, C and L) which are extracted from distributed parasitic parameters
  - A set of active devices
- The active devices are characterized by differential equations where the constituent parameters are variables. This representation is in general non-linear but can be modeled using a piece wise linear technique.

Piece Wise Linear Modeling Advantages

- Piece Wise Linear models for the active devices reduces the computation load for the simulation task.
  - Linearizing the behavior of non-linear devices by regions of operation simplifies the computational task to solve the system.
  - This also allows us to trade accuracy for speed.
- PWL modeling offers reliable performance without the computational load of circuit simulators such as SPICE.
- PWL models for optoelectronic devices allow Chatoyant to integrate electrical and optical components in the same simulation.

Approach

Four steps:

1. Modified Nodal Matrix representation to characterize the system[e.g. J. Vlach, K. Singhai, Computer Methods for Circuit analysis and Design]
2. Linear and non-linear sub-block decomposition
3. Piecewise modeling of active devices for the non-linear sub-block
4. Re-compute and Pre-characterization of the solution caused by changes between piecewise models. These changes depend on the state variables of the network

1 Modified Nodal Matrix Representation

- Characterization of the system using a well-known MNM (Modified Nodal Matrix).

1) $C\dot{v} = -Gv + Bu,$ v – state variables vector

2) $i = L^T v + Du,$ u – source vector

C – storing matrix

G – conductance matrix

B, L, D – mapping matrices

2 Linear and Non-linear Sub-block Decomposition

- Decomposition of the design into a linear multiport sub-block section and a non-linear sub-block.
  - The linear block will characterize the interconnection network.
  - The non-linear sub-block will include the active devices.
- The linear sub-block can be analyzed using a direct and exact solution or any approximation method based in its size.
  - The solution from this block would be a matrix in which elements correspond to the transfer function between a pair of ports in the block.
  - The linear sub-block would then be characterized and able to be used for any subsequent situation in the system.

3 Piecewise Modeling of Active Devices

- Form the non-linear sub-block: A MNA matrix template will be used for each device in the network.

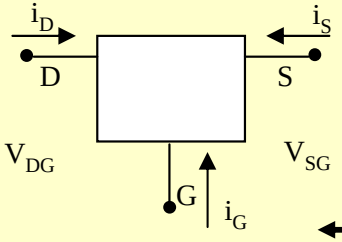
  Example: FET template

$$\underbrace{\begin{bmatrix} (C_{gd}+C_{ds}) & -C_{gd} & -C_{ds} & 0 & 0 & 0 \\ -C_{gd} & (C_{gd}+C_{gs}) & -C_{gs} & 0 & 0 & 0 \\ -C_{ds} & -C_{gs} & (C_{gs}+C_{ds}) & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}}_{C} * \begin{bmatrix} \dot{v}_d \\ \dot{v}_g \\ \dot{v}_s \\ \dot{i}_d \\ \dot{i}_g \\ \dot{i}_s \end{bmatrix} \Big\} \dot{x}_n = -\underbrace{\begin{bmatrix} gds & gm & (-gds-gm) & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 \\ -gds & gm & (gds-gm) & 0 & 0 & -1 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \end{bmatrix}}_{G} * \begin{bmatrix} v_d \\ v_g \\ v_s \\ i_d \\ i_g \\ i_s \end{bmatrix} \Big\} x_n + \underbrace{\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix}}_{B} * \begin{bmatrix} u_d \\ u_g \\ u_s \end{bmatrix}$$

Port Voltages

$$\begin{bmatrix} i_D \\ i_G \\ i_S \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}}_{B^T} * x_n$$

Port currents



FET 3-port model

4 Re-Compute and Pre-characterization

- The use of piecewise models is based on changing models for active devices depending on the change in conditions in the circuit.
- During each new timestep the state variables in the system will change and might cause the active devices to change their modes of operation.
- This process can be simplified if the transfer function between devices (given by the linear block pre-solution) is used as a guide.

Dynamic Sampling Control

- Because of the mixed technology environment of the simulator, multi-rate dynamics have been considered.
- An algorithm to control the sample granularity of the PWL waveform in each module was developed.
- The inclusion of the samples during fast transitions, or suppression of time-points during “steady state” periods optimizes the number used in the simulation.
- The addition of this algorithm allows the creation of Adaptive PieceWise Linear (APWL) modules.

CMOS Inverter Piecewise Models

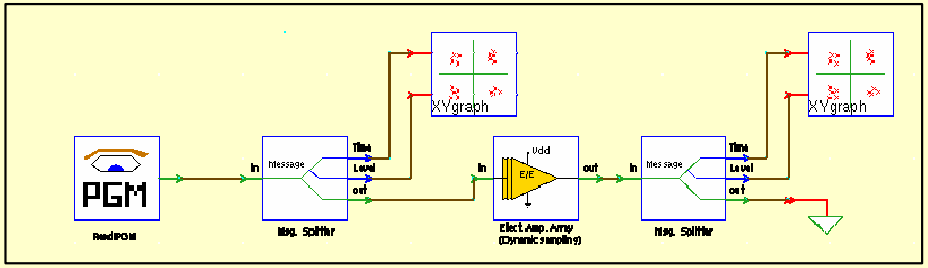
- CMOS inverter modeling as a particular case for the application of piecewise modeling techniques:
  - **Two V-I discrete equations for modeling the behavior of a CMOS inverter after the expanding the macromodel solution.**

$$V_{ds}(t_0+\Delta t)=V_{ds}(t_0)+\frac{I_{dsnet}(t_0)}{g_{ds}(t_0)}\left(e^{\frac{g_{ds}(t_0)\Delta t}{C}}-1\right)+\frac{g_m(t_0)}{g_{ds}(t_0)}\left[\frac{\left(\frac{C_{gd}}{g_m(t_0)}+\frac{C}{g_{ds}(t_0)}\right)}{\Delta t}\left(e^{\frac{g_{ds}(t_0)\Delta t}{C}}-1\right)-1\right]\left(V_{gs}(t_0+\Delta t)-V_{gs}(t_0)\right) \quad \textbf{Model I}$$

$$V_{ds}(t+\Delta t)=V_{ds}(t)+\frac{I_{dsnet}(t)\Delta t}{C-\frac{g_{ds}(t)\Delta t}{2}}+\left[\frac{C_{gd}+\frac{g_m(t)\Delta t}{2}}{C-\frac{g_{ds}(t)\Delta t}{2}}\right]\left[V_{gs}(t+\Delta t)-V_{gs}(t)\right] \quad \textbf{Model II}$$

  - Model I is more stable when the sampling time is larger than the response time of the device [dynamic $\approx C/g_{ds}(t)$].
  - Model II has a better response at the ends of the amplifier dynamic range.
  - The simplicity of model II makes the fitting process easier.

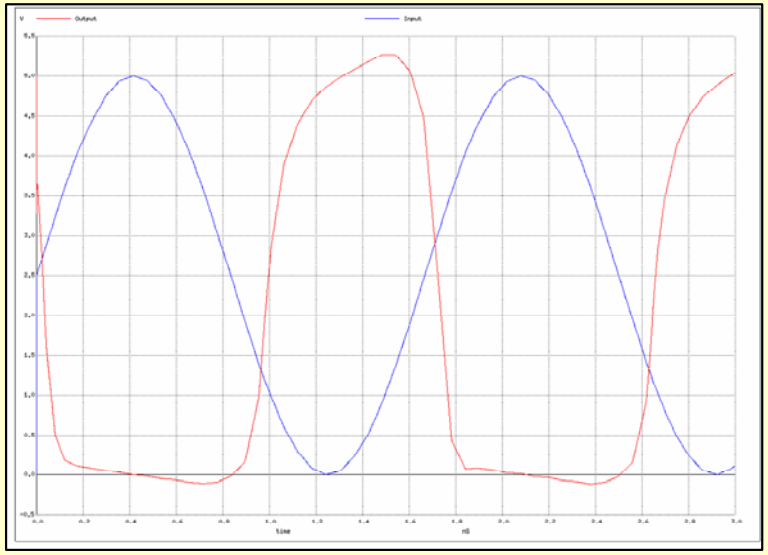
Electrical Driver Modeling



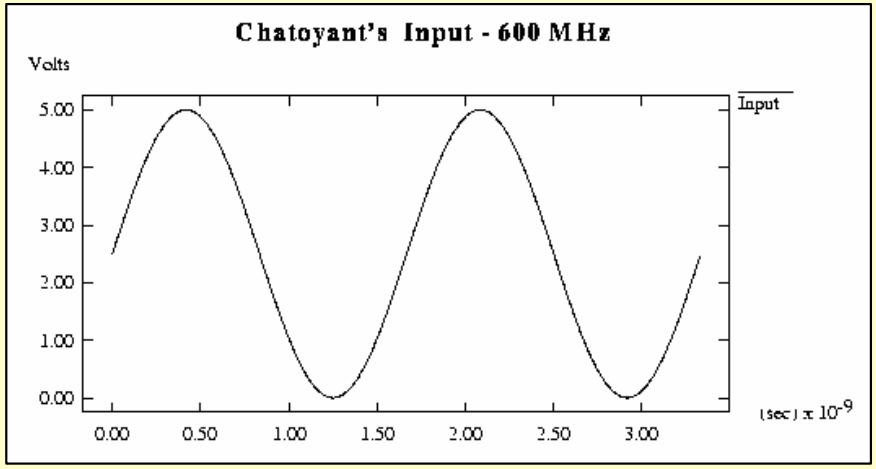
Chatoyant's driver system

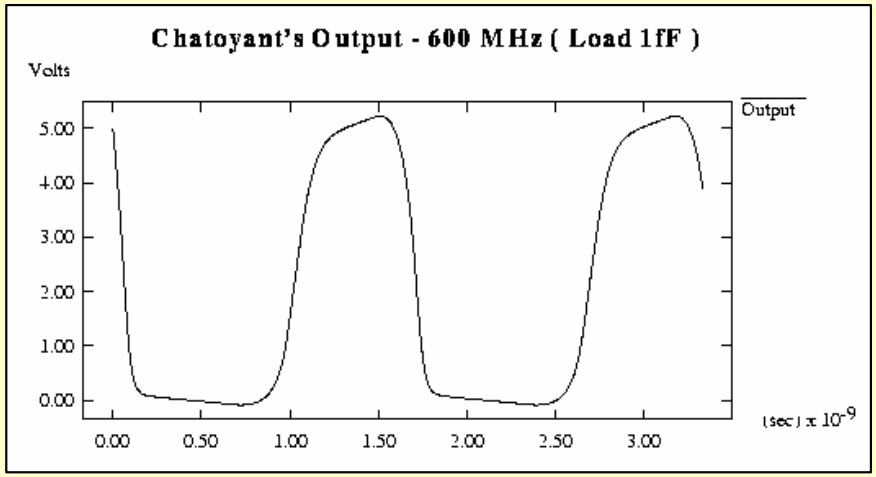
High frequency response in Chatoyant shows a very close match to the SPICE counterpart ($f = 600$ MHz & $C_{ld} = 1$fF).

Input Output



Spice's Response - 600 MHz (Load 1fF)

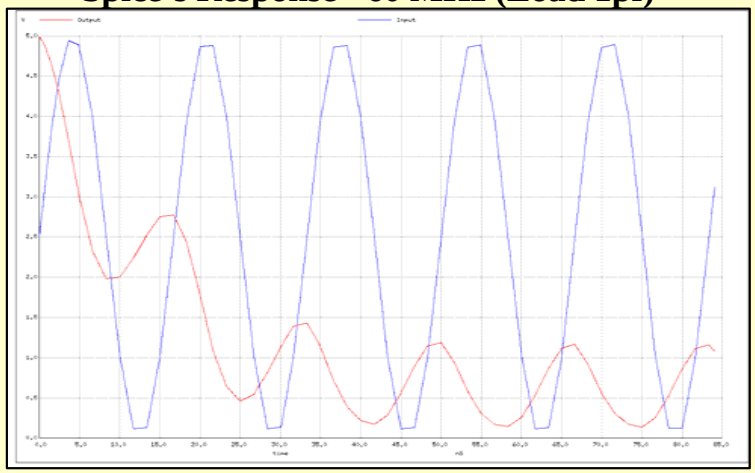




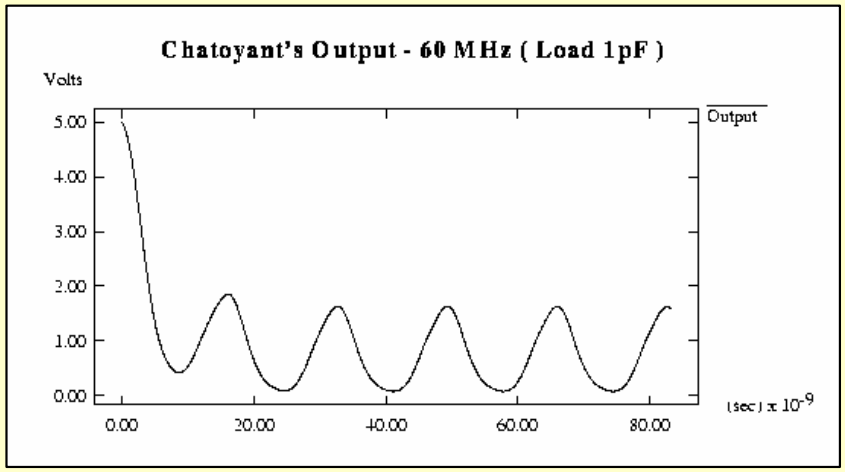
Electrical Drivers, Dynamic effects

High Load Response

Spice's Response - 60 MHz (Load 1pf)

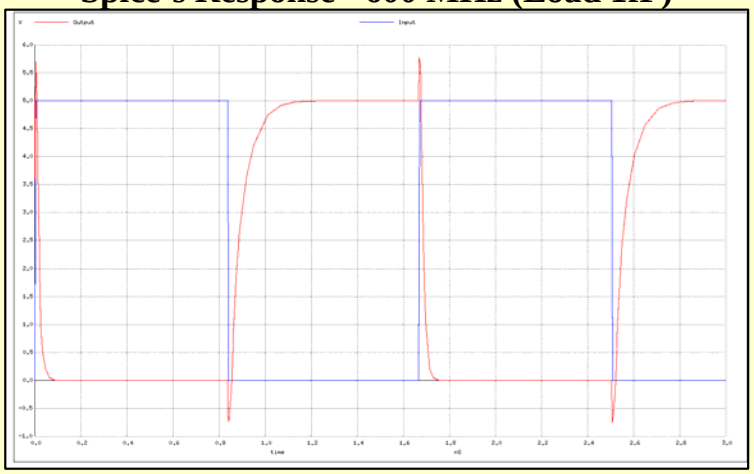


Input Output

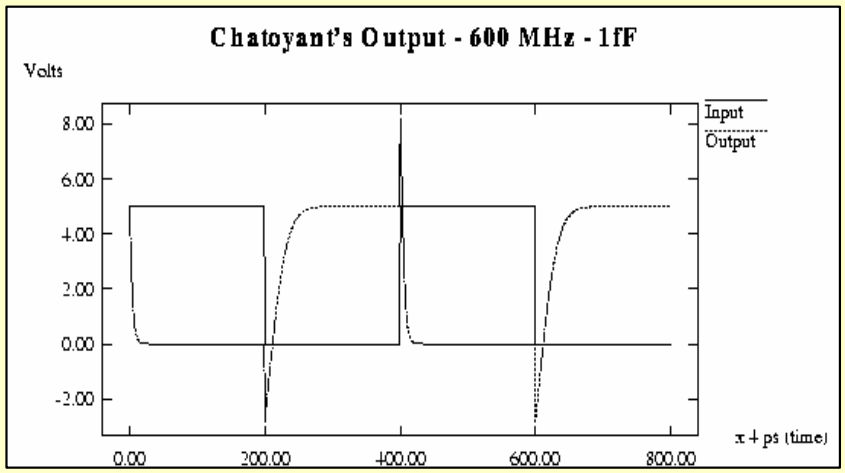


Pulse Response (600 MHz)

Spice's Response - 600 MHz (Load 1fF)

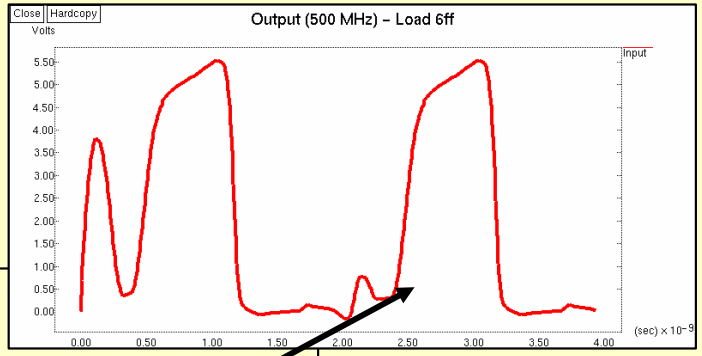


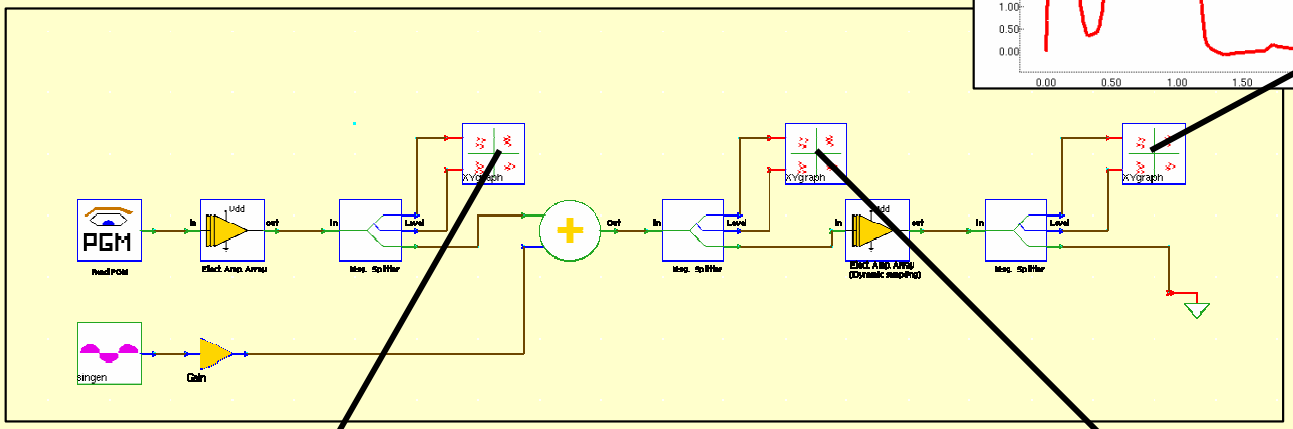
Input Output

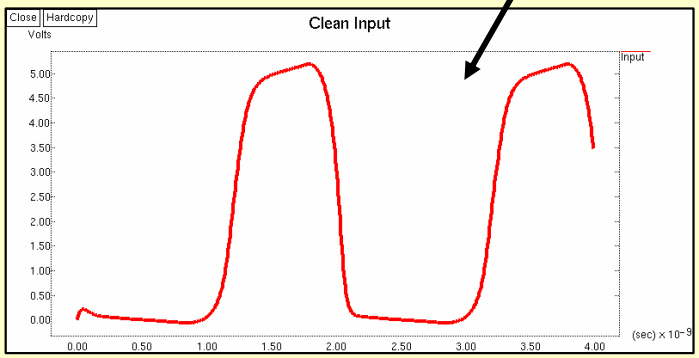


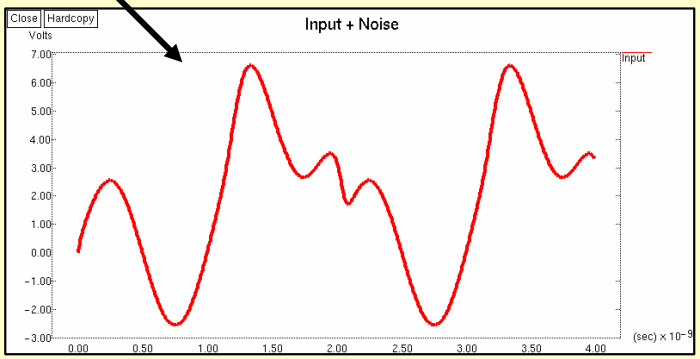
Electrical Drivers, Dynamic effects cont.

- Chatoyant screen shot showing the role of the threshold in the logical detection process of the electrical driver.



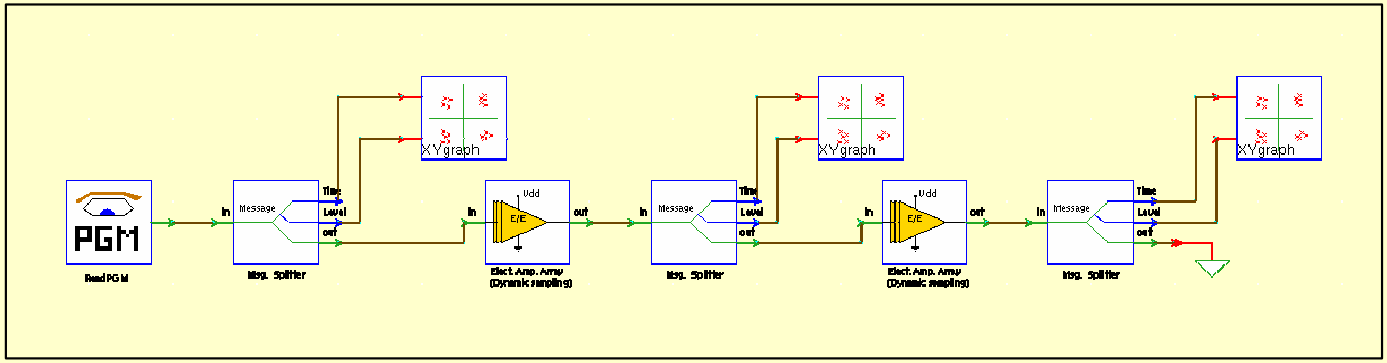


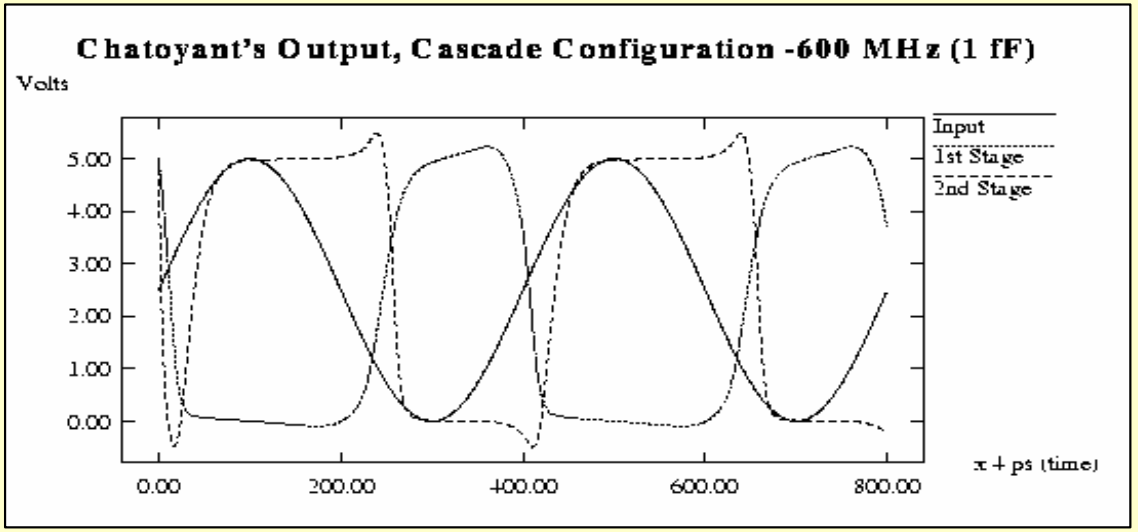




Electrical Drivers in Cascade Operation

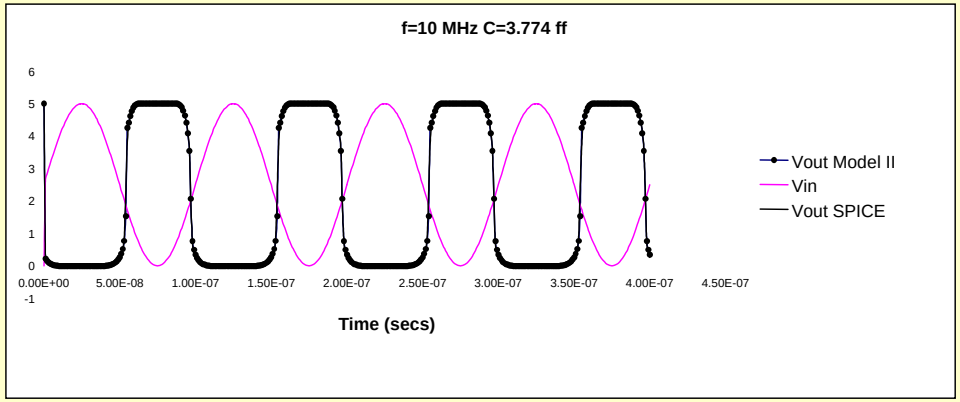
High frequency response in Chatoyant for a cascade driver configuration (f = 600 MHz & C_{ld} = 1fF).

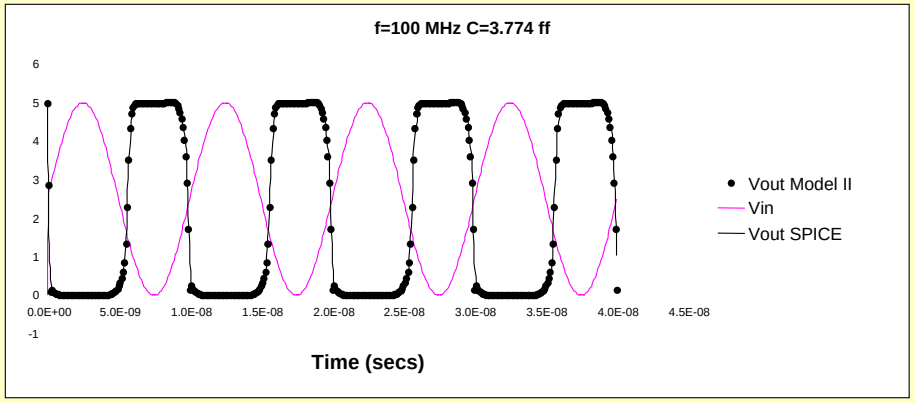


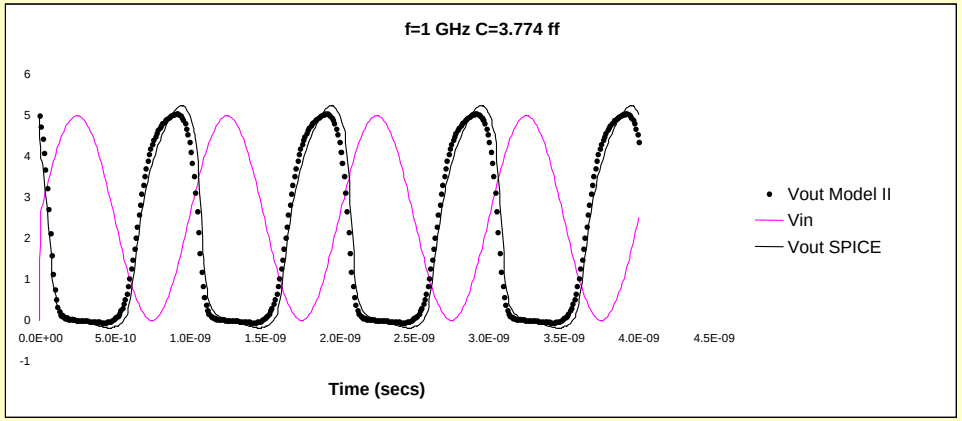


Electrical Driver Models vs. SPICE

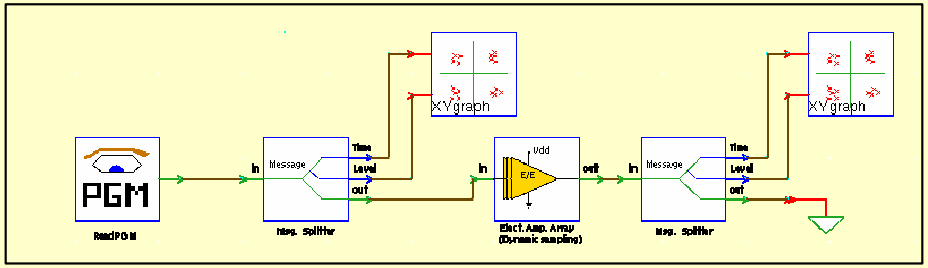
	f= 10 MHz C=3.774ff			f= 100 MHz C=3.774ff			f= 1 GHz C=3.774ff		
	SPICE Level 2	Model I	Model II	SPICE Level 2	Model I	Model II	SPICE Level 2	Model I	Model II
Speed									
Time	0.13	0.093	0.15	0.12	0.089	0.091	0.12	0.094	0.089
Iterations	307	100	200	313	100	100	300	100	100
Accuracy	0	9.1%/18.8 SD	1.8%/4.7 SD	0	3.4%/6.8 SD	3.3%/6.7 SD	0	10%/12.9SD	9.99%/13.8SD



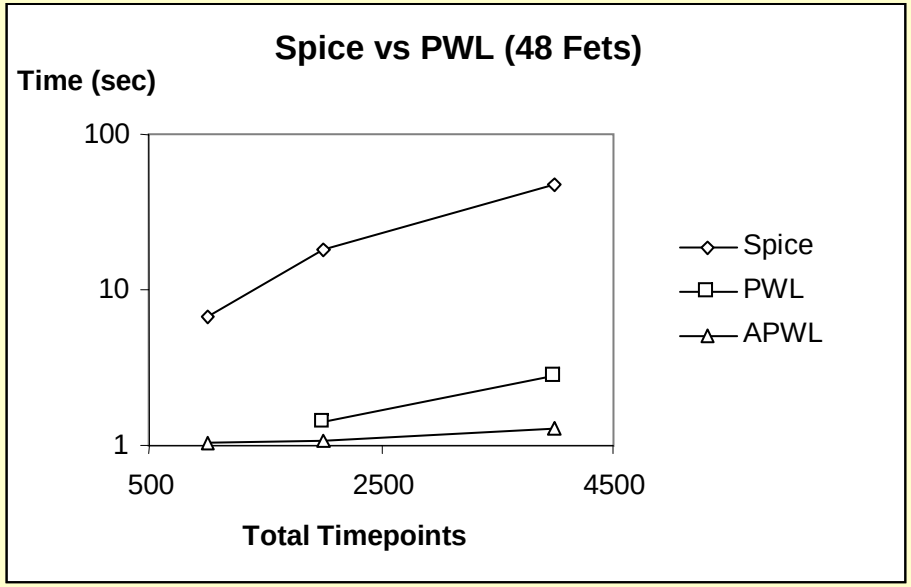


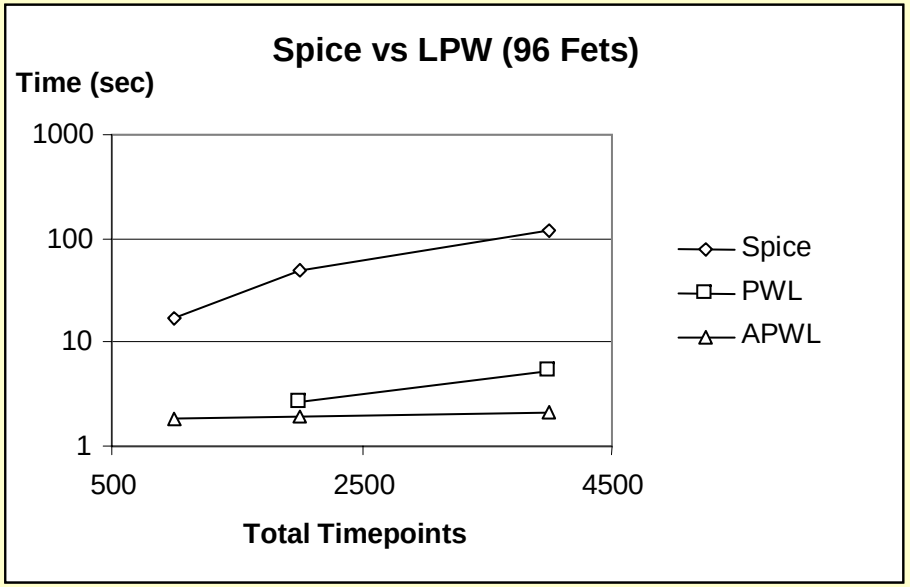


The times for the models include the computational load of the whole system (Chatoyant Implementation).



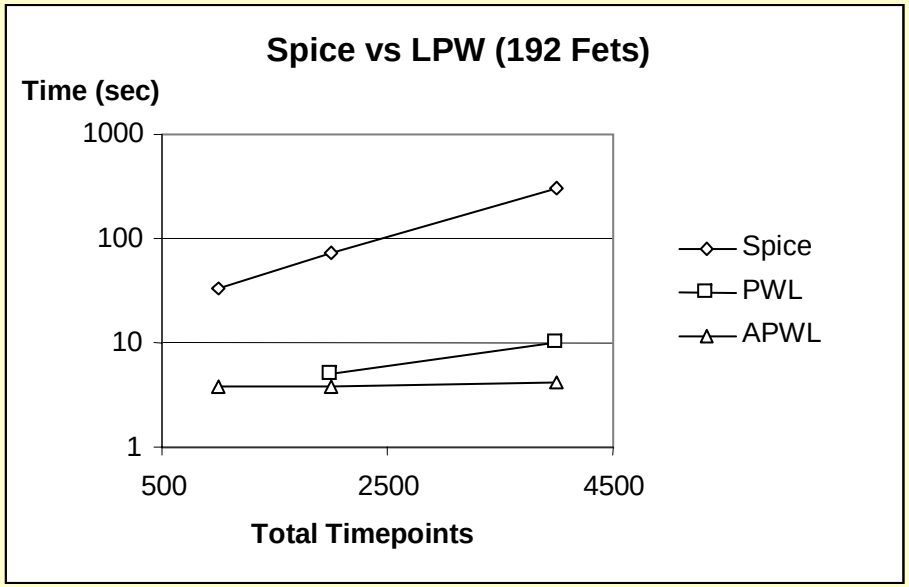
Piecewise Linear Simulation Performance

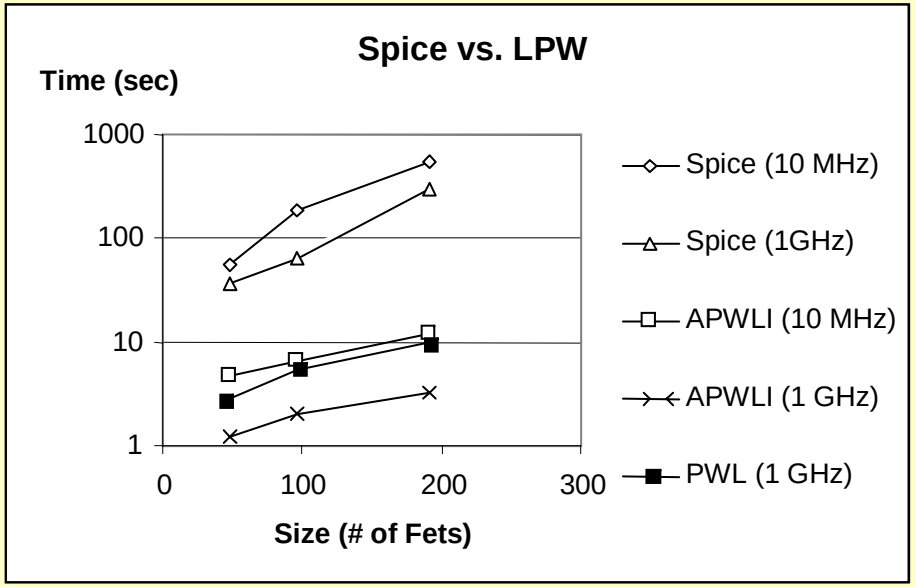




- Spice vs. PWL Models and APWL Models in a system of different sizes (48 and 96 FETs) (f=100/500/1000 MHz).

Piecewise Linear Simulation Performance cont.

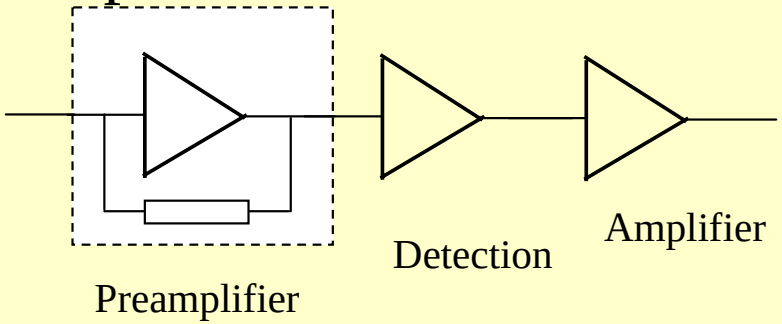




- Spice vs. PWL Models and APWL in a system of multiple gates (f = 100/500/1000 MHz)

Optical Receivers

- In general Optical Receivers can be considered as composed of three basic sections: Preamplifier, Decision-maker or detection and amplifier:



- The Decision-maker and amplifier are generally designed using standard CMOS inverter sections whose large signal models were shown.
- The main difference between these two sections is the type of operation: Small signal operation for the decision-maker and large signal operation for the amplifier. Both of which can be handled using the previous piecewise linear models.

Transimpedance Amplifier Model

- In Optical Receivers the preamplifier section is generally a transimpedance amplifier.
- This configuration provides:
  - Improved linearity
  - Increased operational bandwidth
  - Immunity to fabrication variations
- The preamplifier circuit will be in the small signal operation mode because of the small levels of current from the opto-electronic transceiver. This fact allows us to characterize this section using a small signal model.

$$Acl(\omega) = Acl \cdot \frac{1}{\frac{s^2 + (\omega_{ho} + \omega_{hi} + \frac{\omega_{ho} \cdot \omega_{hi}}{\omega_f} \cdot \beta \cdot Aol)s}{\omega_{ho} \cdot \omega_{hi} \cdot (1 + \beta \cdot Aol)} + 1}$$

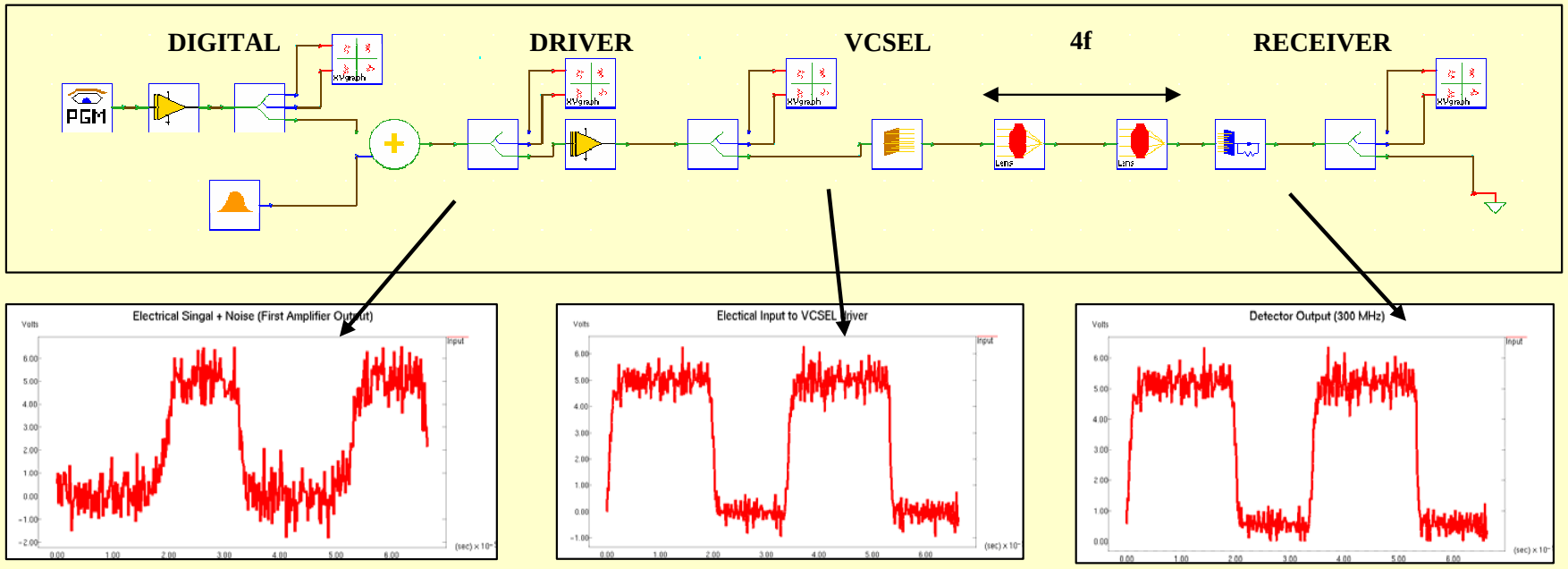
← Transimpedance gain for the preamplifier

Optoelectronics Integration

- Piece Wise Linear modeling technique for electrical drivers, optical receivers (transimpedance type), and general optoelectronic devices (e.g. LCD) allows Chatoyant to integrate electrical and optical components in the same simulation.
- Two examples of integrated electronics and optics system through piecewise modeling:
  - Complete 4f free space optical link
  - A Multi-rate system: 4f free space optical link with a SLM (LCD)

Complete 4f Free Space Optical Link

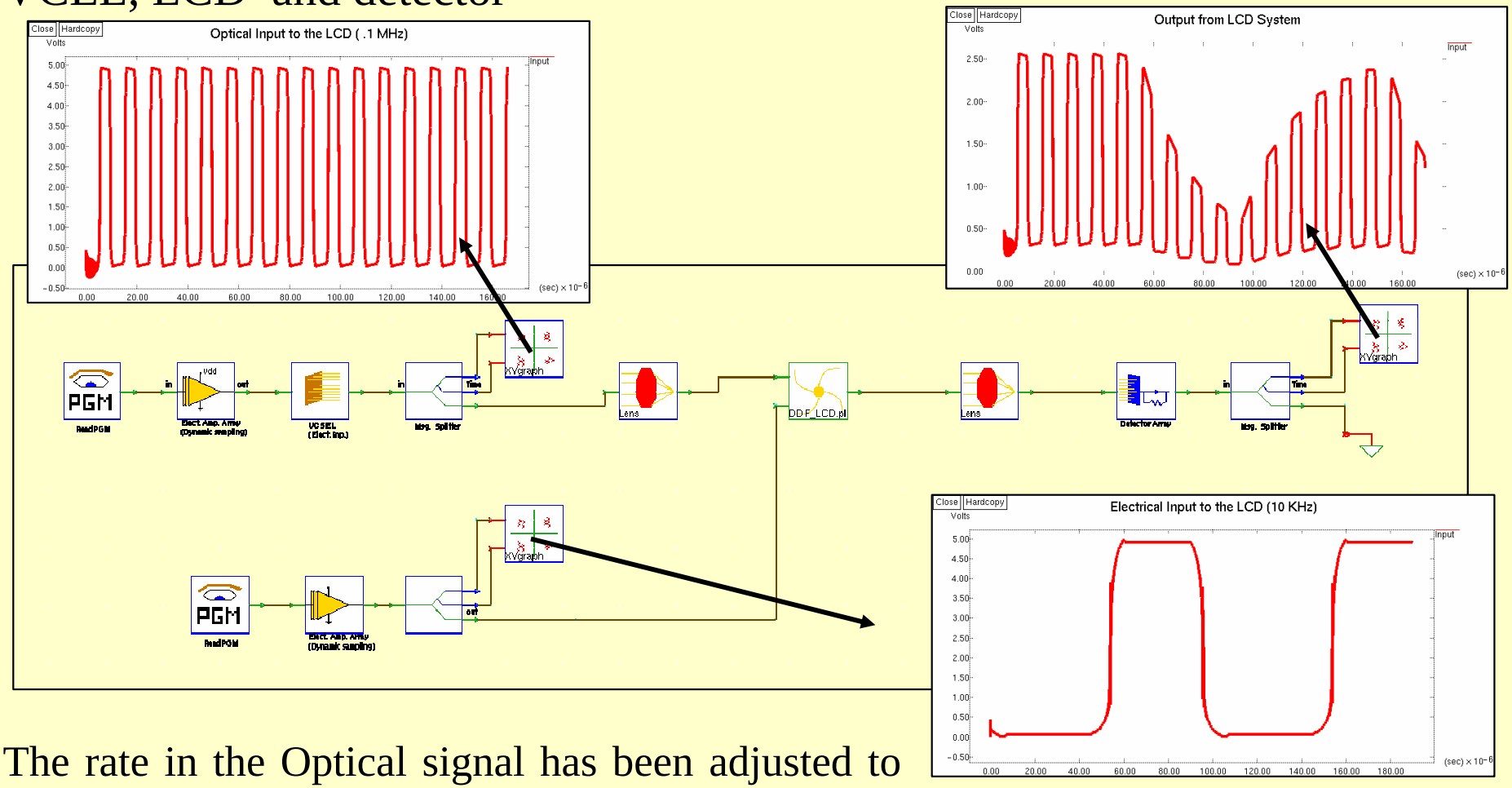
Chatoyant screen shot showing a 4f OE link system including PWL drivers and detector



Gaussian noise has been added to the digital input to analyze the impact of noise on the received signal

A Multi-rate System: 4f Free Space Optical Link with a SLM (LCD)

Chatoyant screen shot showing a 4f OE link system including PWL drivers, VCEL, LCD and detector



The rate in the Optical signal has been adjusted to 100 KHz to show the effect of the response time in the LCD impact in the received signal

Summary

- We presented our piecewise linear models for CMOS circuits. These models are two orders of magnitude faster than SPICE, and have less than 10% absolute error.
- We have incorporated these models into Chatoyant. Using the DDF and DE domains, we have integrated these models into a piecewise linear simulator that is capable of modeling electronic, optoelectronic and optical signals in the same environment.
- The ability of these models to respond to arbitrary waveforms allows us to perform system level modeling including cross-talk, noise and bit error rate calculations in a discrete event simulation framework.

Future Work

- Use of piecewise modeling technique on more optoelectronic circuits (e.g., complex CMOS logic circuits).
- Comparison with experimental data from real circuits in test chips [e.g., OThB2, Thursday 11:00 am]
- Use of approximation methods to compute the solution of MNA for large circuits [PVL "Pade via Lanczos" or any efficient algorithm to compute Pade approximation]

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