Three-dimensional integrated circuits for lab-on-chip dielectrophoresis of nanometer scale particles

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ABSTRACT

In this paper, we present a mixed-technology micro-system for electronically manipulating and optically detecting virus-scale particles in fluids that is designed using 3D integrated circuit technology. During the 3D fabrication process, the top-most chip tier is assembled upside down and the substrate material is removed. This places the polysilicon layer, which is used to create geometries with the process' minimum feature size, in close proximity to a fluid channel etched into the top of the stack. By taking advantage of these processing features inherent to "3D chip-stacking" technology, we create electrode arrays that have a gap spacing of 270 nm. Using 3D CMOS technology also provides the ability to densely integrate analog and digital control circuitry for the electrodes by using the additional levels of the chip stack. We show simulations of the system with a physical model of a Kaposi's sarcoma-associated herpes virus, which has a radius of approximately 125 nm, being dielectrophoretically arranged into striped patterns. We also discuss how these striped patterns of trapped nanometer scale particles create an effective diffraction grating which can then be sensed with macro-scale optical techniques.

Keywords: Dielectrophoresis, 3D integrated circuits, lab-on-chip

1. INTRODUCTION

Labs-on-chips, similar to systems-on-a-chip, attempt to offer complete economical solutions for biomedical applications. Labs-on-chips combine, in monolithic form, sample containment, transportation (microfluidic), programmability, and detection for bio-sensing [1]. Lab-on-chip miniaturization advantages include not only sample consumption reduction but also greater resolution for bio-sensing.

Dielectrophoresis has been used in a broad range of lab-on-chip applications such as cytometry, cell sorting and mixture separation. Due to technology limitations, most implementations are restricted to fabricating dielectrophoresis electrodes that are on the micron scale and therefore it is impractical to implement a system that can manipulate nanometer scale particles such as viruses using an integrated circuit process. This paper shows how a lab-on-chip that uses dielectrophoresis to manipulate nanometer scale particles can be designed by taking advantage of fabrication features found in 3D integrated circuit technologies. For 3D chip fabrication, the top tier in the vertical stack of chips is upside down with respect to its normal orientation and the layers associated with it, normally at the bottom of a conventional chip, are now located towards the top surface of the 3D chip. This closeness to the surface allows the layer with the smallest realizable feature size for the technology, the polysilicon layer, to be used for the design of electrodes.

Three dimensional integrated circuits are a promising platform for lab-on-chip applications because these types of microsystems usually consist of digital elements, such as microcontrollers and memories, and analog circuits that act as an interface to a transducer. Often, manufacturing all of these components on a single chip is either impossible or much more expensive than putting them on multiple chips. Fabricating labs-on-chips using a 3D process allows manufacturers to take advantage of the same benefits that are inherent to conventional 3D chips, such as a reduction in average interconnect length[2]. In many instances, such as the lab-on-chip presented in this paper, the transducers are placed in very large arrays [3], [4]. As these arrays become more and more dense, they become more difficult to floorplan and route. When labs-on-chips are designed in a 3D integrated circuit process, the main partitions of the microsystem can be separated onto different chip tiers, simplifying the routing problem by allowing the necessary support circuitry for each transducer element to be placed directly under it, requiring only a short vertical inter-tier via for interconnect.

The rest of the paper is organized as follows: A detailed description of the chip's architecture and fabrication steps is provided in section 2. Section 3 gives a theoretical background of dielectrophoresis and discusses some of the issues

that arise when dielectrophoresis is used to control nanometer scale particles. Section 4 demonstrates with simulations how this microsystem can be used to manipulate virus particles. Section 5 shows how the particles can be arranged to form diffraction grating structures such that their presence can be optically detected. Section 6 contains a summary of the work presented in this paper.

2. DESIGN OF 3D LAB-ON-CHIP

2.1 3D lab-on-chip fabrication

The lab-on-chip described in this paper is fabricated using MIT Lincoln Labs 3D, 0.18um, silicon-on-insulator (SOI) technology [5]. For this integrated circuit process, three dimensional circuit structures are formed by transferring and interconnecting conventional silicon wafers in a vertically tiered fashion. In this process there are three tiers that consist of layers for interconnect and active silicon. The 3D integration process begins with the fabrication of three fully depleted SOI tiers. The handle silicon is removed from the second tier which is then turned upside down and bonded to the first wafer tier. The third tier is transferred to the two-level stack using the same processing steps as for the second tier. Three-dimensional vias are etched through the oxide layers of the tiers and filled with tungsten. As shown in figure 1, the resulting chip has three levels of active devices with each layer providing metal horizontal interconnect and vertical inter-tier vias.

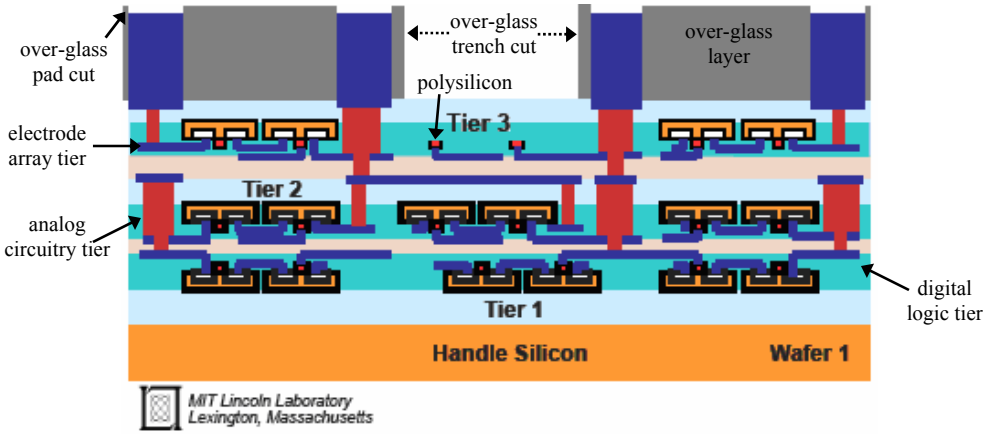

Fig. 1. Cross section of 3D chip stack (Courtesy of MIT Lincoln Laboratory, used with permission). Displayed on each chip tier are the active silicon and interconnect layers. The center over-glass cut is an example of how the over-glass layer can be used to form fluidic trenches. Figure not drawn to scale.

2.2 Chip architecture

The three dimensional chip stack, as shown in figure 1, is organized as follows: the topmost chip tier, tier three, is used for the polysilicon electrode array. The voltage on each electrode is individually driven by analog circuitry on the middle tier. The bottom tier, tier one, contains the digital circuits that are necessary to select the waveform on each electrode.

Two 1,000um x 200um pad cuts are made through the top over-glass layer, located on the surface of the chip. The areas of top level metal that would normally be used for contact pads are chemically etched away within this region to form trenches, as seen at the top of the chip cross section shown in figure 1. These fluidic trenches are used to hold a buffer solution that contains the particles of interest. Because the topmost chip tier in this 3D process is assembled upside down, the active devices within this tier are located in very close proximity to the top surface. This enables the polysilicon layer that is normally used as interconnect for active circuit devices, to be used to create dielectrophoresis trapping electrodes. This would not be possible using a conventional integrated circuit process, as this layer would be at the bottom of the chip.

Using the polysilicon layer to form electrodes yields several advantages. First, structures with the minimum possible feature size in an integrated circuit process can be realized by using the polysilicon layer. This design technique is used to form a linear array of 2,048 DEP electrodes each being 180 nm wide and 200 um long, resulting in an electrode array under the trench area with a center to center pitch of 450 nm and an electrode gap spacing of 270 nm. Second, the polysilicon layer is at the lower levels of the chip fabrication process which puts it at the top of the assembled 3D chip

stack. The electrodes are separated from the bottom surface of the trench by 650 nm of oxide. Figure 2 shows a 3D depiction of the lab-on-chip and close up view of the electrode array. As explained in section 3 of this paper, an electrode array with such a fine pitch yields a high degree of selectivity when manipulating submicron size particles. This is a large reduction in electrode feature size when compared to most DEP based microsystems implemented using integrated circuit technologies. Those systems are only able to form trapping electrodes using the top metal layers normally reserved for bonding pads, and are on a scale ranging from a few to tens of microns [3],[4].

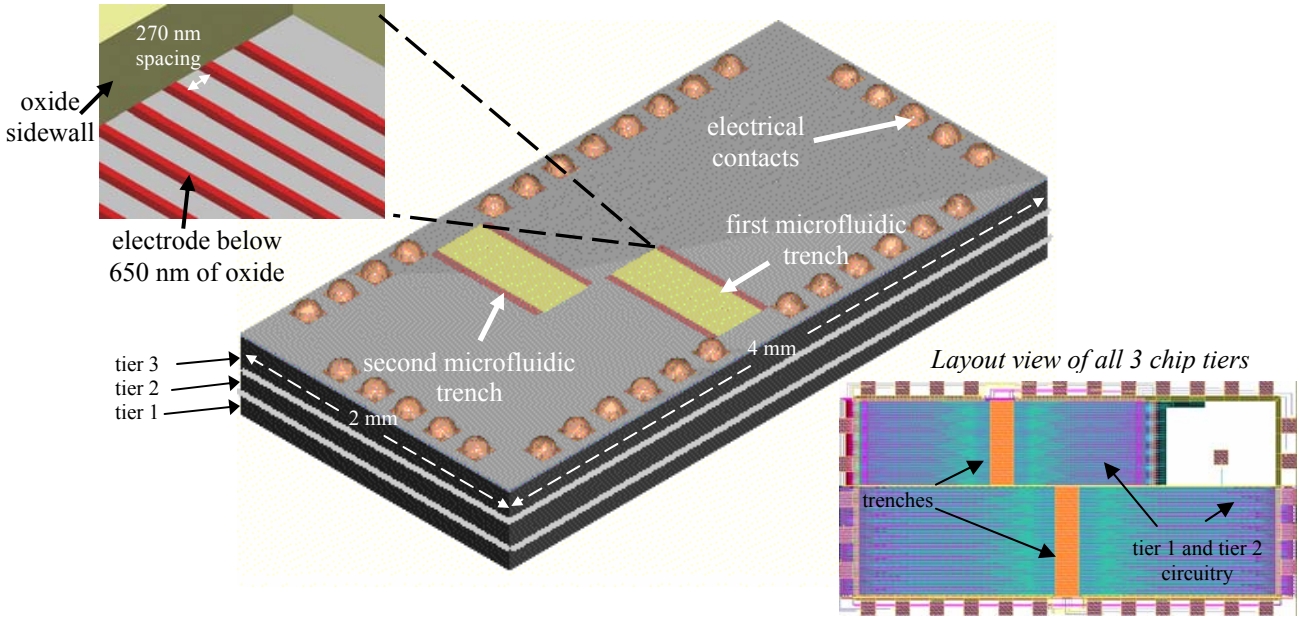

Fig. 2. Physical layout of 3D lab-on-chip. The top tier is used for fluid trenches and polysilicon electrodes. Analog and digital circuitry is located on the middle and bottom chip tiers. Inset at top shows a close-up of the polysilicon electrodes. The bottom inset shows a superposition of the VLSI layout of all three chip tiers.

The electronic design of the chip is based on a set of control registers for each of the 2,048 electrodes that are used to select among four source waveforms provided externally to the chip. The block diagram in figure 3 shows how the analog selector circuits are controlled digitally. The select input of each analog mux is driven by a 2-bit wide, 4-bit deep circular shift register. The shift registers have two modes, load and circulate. In order to minimize the number of I/O pins necessary for loading, the output of the last register in each row is fed to the input of the subsequent row. Once the time sequenced pattern for each row has been initialized and the chip placed into circulation mode, the signal on the electrode can switch between one of four analog inputs on every clock cycle. This architecture provides flexibility for post-fabrication experimentation, as the design is not limited by waveforms that are only generated on chip. The left hand side of figure 4 shows the schematic of the analog multiplexer that selects the signals for the electrodes. The waveform on the right of figure 4 shows a simulation of 4 separate muxes switching the waveform on 4 separate electrodes on the rising edge of every clock cycle.

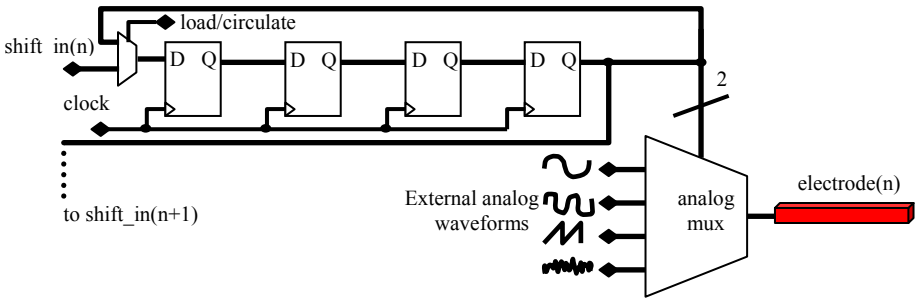

Fig. 3. Block diagram of circuitry used to control each electrode. The circular shift register selects which of the four external waveforms will appear on the electrode. The output of the shift register is also used as the input to the shift register on the successive row when initializing the selection pattern.

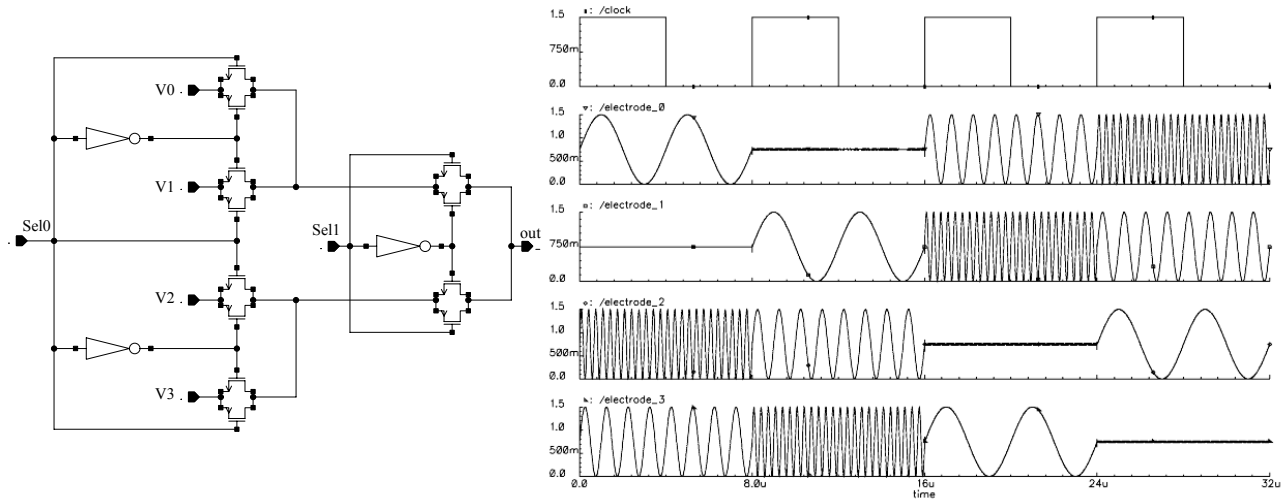

Fig. 4. The left shows one of the 4:1 analog multiplexers, on the right are simulation results of four such muxes switching the waveform on four separate electrodes on the rising edge of every clock cycle.

3. DIELECTROPHORESIS OF NANOMETER SCALE PARTICLES

Dielectrophoresis is the physical phenomenon whereby dielectric particles, in response to a spatially nonuniform electric field, experience a net force directed toward locations with increasing or decreasing field intensity according to the physical properties of the particles and medium in which they reside [6]. Dielectrophoresis has been shown to be a viable technique for manipulation and trapping of objects on the nanometer scale without the need for contact [7]. When an electrically neutral particle is placed in between a set of electrodes configured to create a nonuniform electric field, the particle becomes polarized, thereby inducing a dipole moment. The average net force exerted on the particle due to the dipole moment is given by:

$$\left\langle \vec{F}_{DEP} \right\rangle = 2\pi\varepsilon_m r^3 \,\mathrm{Re}\left[K_{CM}\right]\nabla E_{rms}^2 \tag{1}$$

$$K_{CM} = \frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_p^* + 2\varepsilon_m^*} \tag{2}$$

$$\varepsilon_{p,m}^* = \varepsilon_{p,m} - \frac{j\sigma_{p,m}}{\omega} \tag{3}$$

where ε_p^* and ε_m^* are the complex permittivities of the particle and the medium, σ is conductivity, r is the radius of the particle and E is the surrounding electric field with an angular frequency of ω. It can be observed from the above equations that the direction of the force vector is independent of the polarity of the electric field. The particle undergoes what is known as positive dielectrophoresis (pDEP) [8] when $\mathrm{Re}[K_{cm}]$, also known as the Clausius-Mossotti factor, is positive. While undergoing positive dielectrophoresis, the force vector is directed along the gradient of electric field intensity and the particles are attracted to the electric field magnitude maxima and repelled from the minima. The opposite occurs when $\mathrm{Re}[K_{cm}]$ is negative. The particles undergo negative dielectrophoresis (nDEP) and are repelled from the maxima and attracted towards the minima.

While equation (1) gives insight on how the particle interacts with its medium, it should be noted that it is a derivation of force based on the assumption that the electric field does not change significantly over the length of the particle [10]. This assumption is not valid when the radius of the particle is on the same order of magnitude as the gap spacing between trapping electrodes. If they are similar in dimension, a more rigorous analysis such as the finite-element method is required to accurately predict values of the dielectrophoresis force vector.

Dielectrophoresis requires an increase in electric field intensity as the radius of the particle decreases. As seen in equation (1), the volume of the particle is directly proportional to the magnitude of the dielectrophoretic force. Therefore, as the particle's size decreases, the dielectrophoretic force exerted on the particle decreases. In order to capture a nanometer scale particle, the electric field strength has to be maximized by means of designing electrode arrays with the minimum possible gap spacing between adjacent electrodes and placed as close to the fluid medium as possible [7].

Since the particles move in an aqueous solution, the opposing hydrodynamic drag force also has to be taken into consideration [9]. Nanometer scale particles have a very small Reynolds numbers, thus the frictional force they experience while moving through fluid can be described by Stokes' law,

$$\vec{F}_{drag} = -6\pi r \eta v \tag{4}$$

where r is the radius of the particle, η is the fluid viscosity and v is the particles velocity. When only the dielectrophoretic and drag forces are taken into consideration, the total net force acting on the particle is given by

$$\vec{F}_{net} = \left\langle \vec{F}_{DEP} \right\rangle - \vec{F}_{drag} \tag{5}$$

The drag force slows the motion of the particles significantly and therefore it is necessary to include it when simulating the movement of the particles in a fluid medium, as is done for the simulations presented in section 4.2.

4. MANIPULATION OF KAPOSI'S SARCOMA-ASSOCIATED HERPES VIRUS

4.1 Electrical modeling of Kaposi's sarcoma-associated herpes virus

Kaposi's sarcoma-associated herpes virus (KSHV) is a recently discovered DNA virus that causes disease in humans and animals. It is of interest to researchers because it is an example of a virus that can cause cancerous tumors. The study of KSHV allows researchers to form a link between the structure of tumor viruses and modern cancer biology [11]. For this reason, it is one of the most interesting subjects in current molecular virology research. KSHV is a spherical virion that has a diameter of approximately 250nm. Its extremely small size creates the need for instrumentation, such as the microsystem presented in this paper, that will allow researchers to manipulate the particles in a consistent and controlled manner.

Previous research has shown the use of dielectrophoresis to manipulate herpes simplex virions [12]. Since KSHV is very similar in its physical structure to HSV, the same electrical model was used for this work. The virion's physical structure is modeled as multiple concentric shells, as depicted in figure 5. The outside layer is an insulating shell, referred to as the lipid bilayer. That shell encloses a thick conductive gel called the tegument. The dielectric properties of the tegument were modeled as having a conductivity of 100 mSm^{-1} and permittivity of $75\varepsilon_0$ while the lipid bilayer was modeled as having a surface conductance of 0.3 nS and permittivity of 7.5ε0.

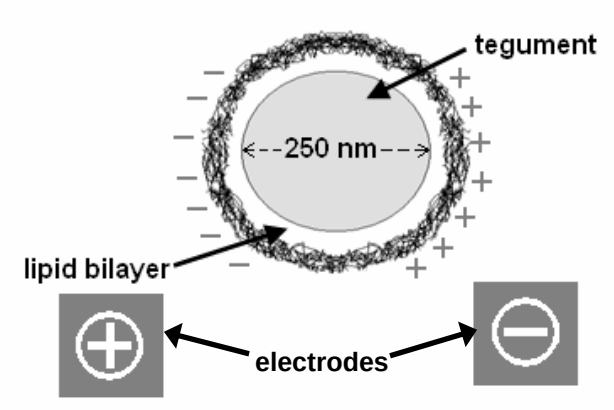

Fig.5. Cross section of Kaposi's sarcoma-associated herpes virus model placed in between two electrodes. Under these conditions the dielectric particle becomes polarized, inducing a dipole moment within the virion that exerts force on the particle.

4.2 Simulation results

Figure 6 shows the results of a 2D finite-element analysis of the electric field generated within the fluidic trench by the electrodes and the resultant dielectrophoretic forces that act on the particles. In this simulation, the first five electrodes, starting from the left of figure 6, are assigned a magnitude of 1.5V. The voltages on the remaining electrodes, on the right hand side of figure 6, are set 180^{o} out of phase with respect to the other electrodes. This creates an electric field maxima between the 5th and 6th electrode. The arrows in figure 6 show the direction of the dielectrophoretic forces that act on the particles as a function of their location within the trench. For this simulation, the particles are more polarizable than their surrounding medium, yielding a positive value for Re[K_{cm}] and the particles within the buffer solution are attracted towards the electric-field maxima.

Experimental results [13] show that when HSV virions are placed in a mannitol solution with a conductivity of 5 mSm^{-1}, the particles will transition from undergoing positive to negative dielectrophoresis in the frequency in the range of 4-5 MHz.

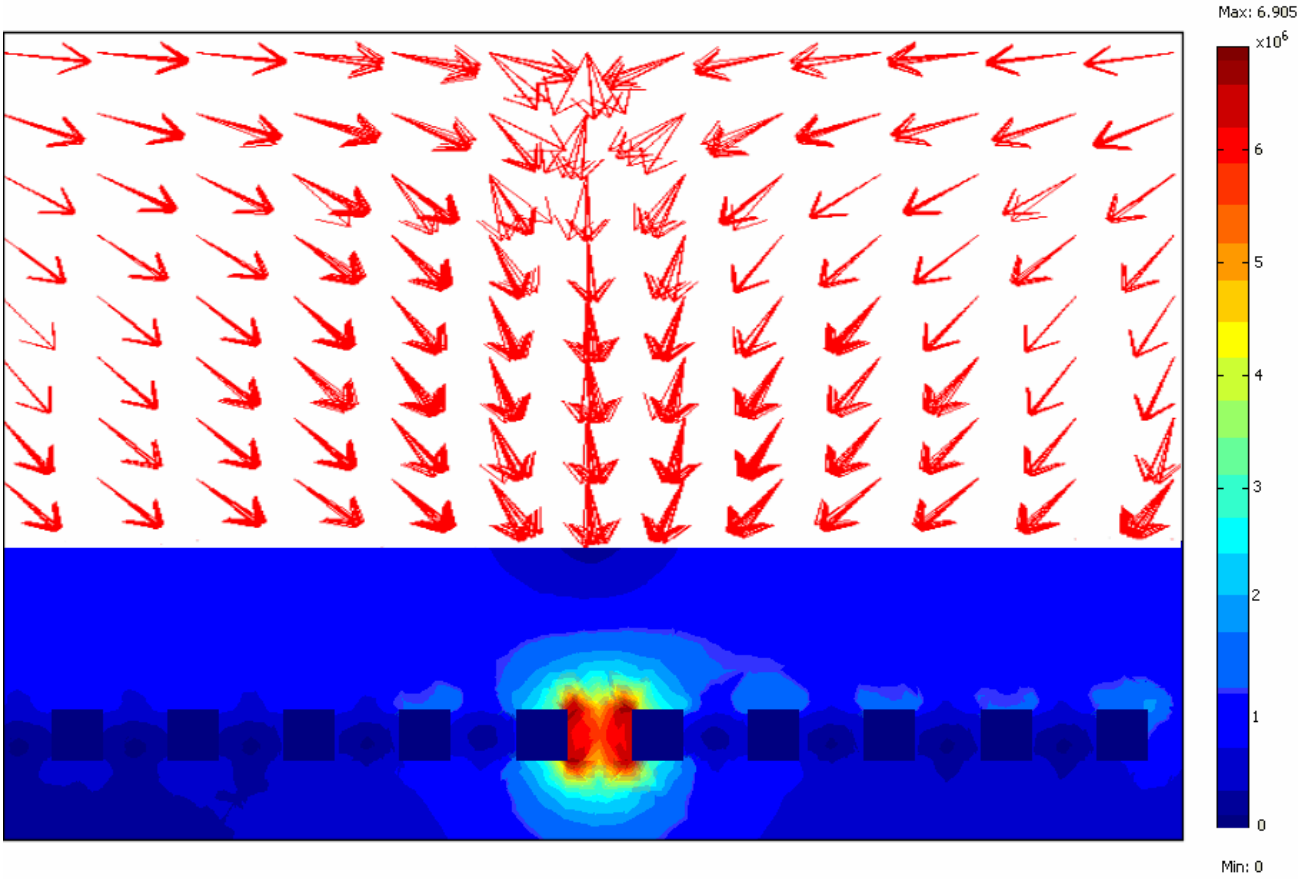

Fig. 6. Finite element analysis of electric field and resulting dielectrophoresis force vectors due the voltage on the center two electrodes being out of phase with each other.

Figures 7(a) through 7(d) show the results of a simulation of a 4um x 25um area of the fluidic trench in which a large concentration of virions are randomly placed. The voltages are set such that each electrode is 180^{o} out of phase with respect to its two neighboring electrodes, creating an alternating pattern of electric field minima and maxima along the bottom surface of the trench. The results of the finite element analysis shown in figure 6 are back annotated into a particle motion simulator and the movement of the virions while under the influence of hydrodynamic drag forces is observed. Figure 7(a) shows the distribution of the particles at time t=0s. As seen by Figure 7(d), the particles reach their steady-state by t=5s and remain trapped after that.

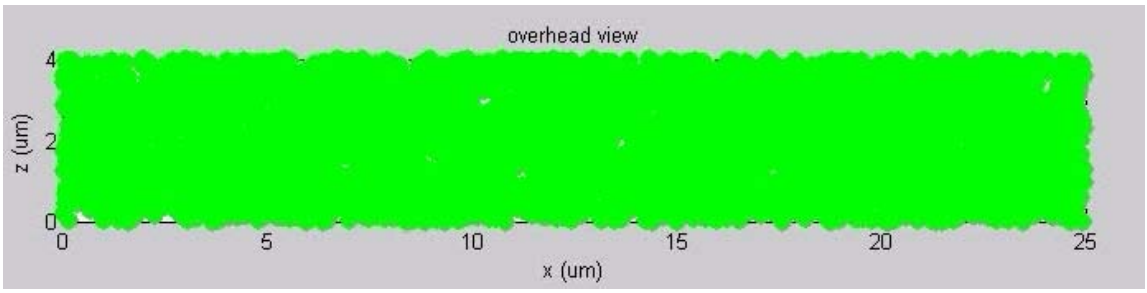

Fig. 7(a). Particles position at t = 0s.

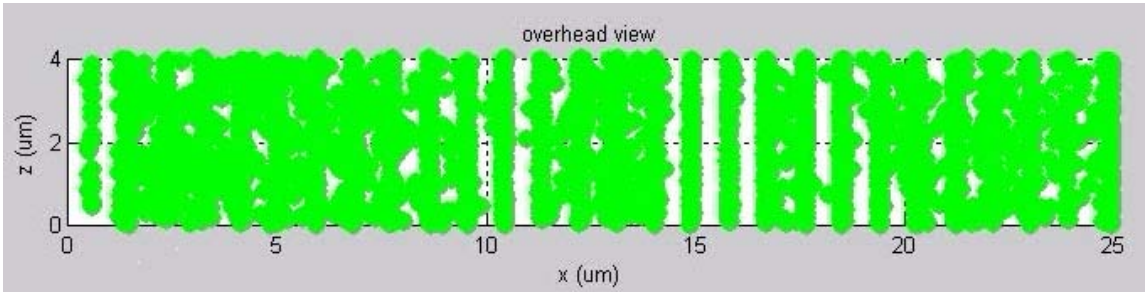

Fig. 7 (b). Particles position at t = 1.5s.

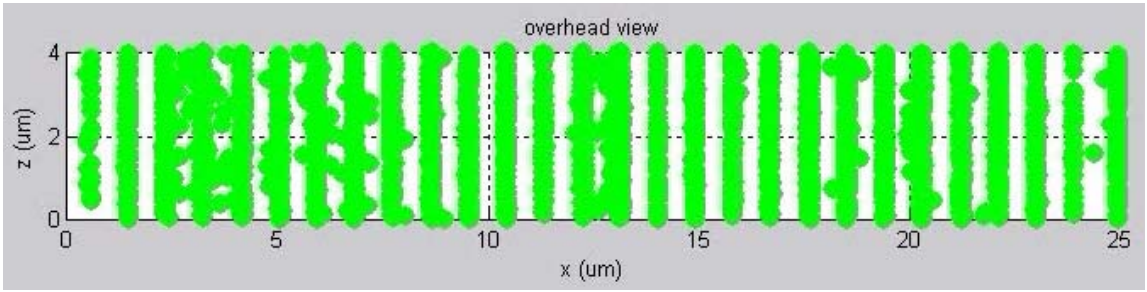

Fig. 7 (c). Particles position at t =3s.

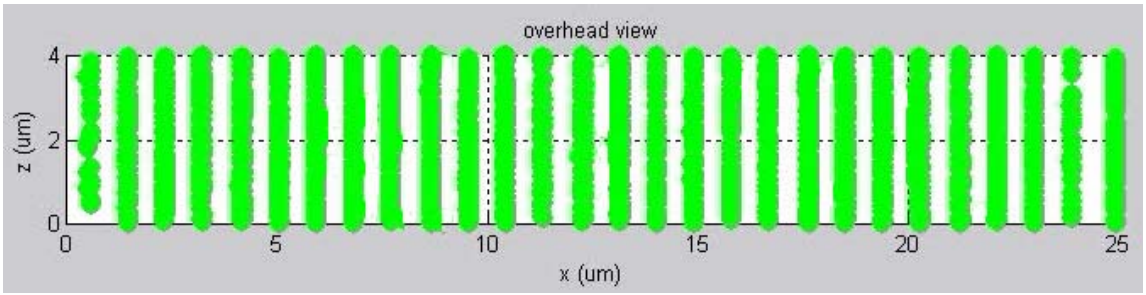

Fig. 7 (d). Particles position at t = 5s.

5. OPTICAL DETECTION OF TRAPPED PARTICLES

A diffraction grating is a reflecting or transparent element whose optical properties are periodically modulated [14]. They are commonly realized as parallel and equally spaced grooves on a material surface. The simulations of section 4.2 show how the lab-on-chip can be used arrange particles into a structure of this form. Figure 8 shows a cross section of the chip when each of the electrodes alternate in phase and the particles are trapped in a line within the gap spacing, as in figure 7(d). For a groove spacing d and a wavelength λ incident at angle β, the grating equation given by:

$$m\lambda = d\left(\sin\theta + \sin\beta\right) \tag{6}$$

gives the value of the diffracted angle θ at which constructive interference will occur in the m[th] diffractive order. If it is assumed that the particles being trapped are opaque and the bottom surface of the chip's trench is made to be reflective, the intensity of diffracted light as a function of its angle of observation angle is:

$$I(\theta) = I_0 \left[sinc\left(\frac{\pi d}{\lambda} \sin\theta \right) \right]^2 \cdot \left[\frac{\sin\left(\frac{N\pi a}{\lambda} \sin\theta \right)}{\sin\left(\frac{\pi a}{\lambda} \sin\theta \right)} \right]^2 \tag{7}$$

where I_0 is the measured intensity for the single slit diffraction case, a is the center to center pitch of the trapped particles and N is the number of grating slits that are illuminated. Figure 9 shows an example of the distribution of diffracted light when a 400nm source illuminates 2,048 grooves of particles that are 250 nm in diameter and are trapped at a pitch of 450nm. The creation of this diffraction pattern allows the presence of particles to be sensed using macro-scale optical detectors, alleviating the need for submicron detection techniques.

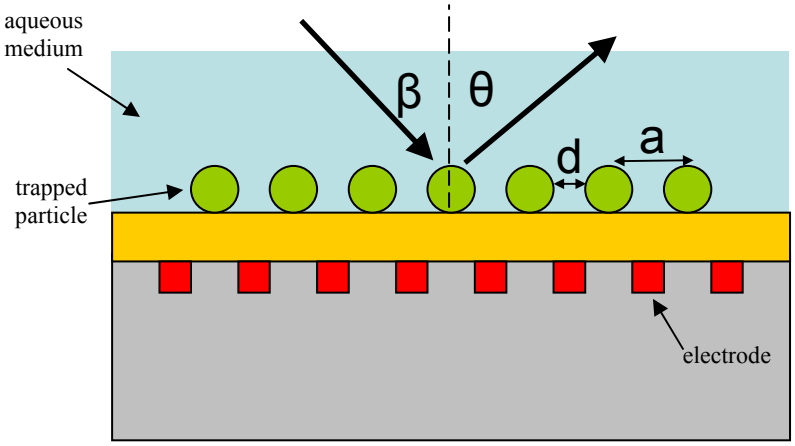

Fig. 8. 2D cross section of dielectrophoretically trapped particles arranged to form a diffraction grating

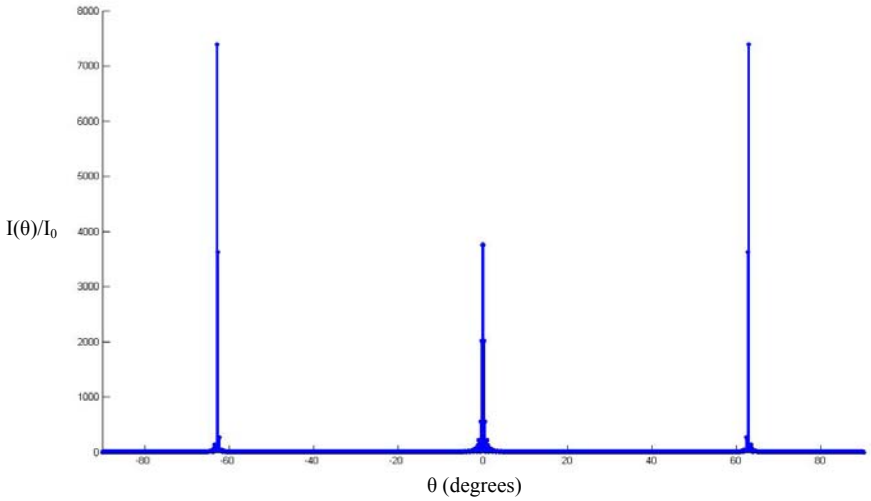

Fig. 9. Distribution of light intensity diffracted by grating formed of particles trapped by dielectrophoresis with d=250 nm, a = 450 nm, N = 2,048 and λ=400 nm

6. SUMMARY

This paper presents the design of a 3D lab-on-chip that uses dielectrophoresis to manipulate nanometer scale particles and shows the benefits of 3D integrated circuit technology when applied to the design of labs-on-chips. Simulations demonstrate how the system can be used to manipulate virus particles and calculations show how the lab-on-chip can arrange particles into a diffraction grating structure that can be detected optically. The dimensions of the lab-on-chip and the dielectrophoresis electrodes are summarized by table 1.

Technology	3D SOI 0.18 um, 3 metal layers/tier
Power Supply	1.5 V
Die Size	2 x 4 mm^2
Num. trapping electrodes	2,048
Electrode gap spacing	270 nm
Electrode center to center pitch	450 nm

Table 1. Summary of chip and electrode dimensions

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