Smart Optical Transceiver Architecture with Dynamic Channel Encoding

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Abstract: In this paper we introduce a novel dynamic channel coding technique designed to minimize errors introduced by electrical noise in the driver and receiver circuits and by channel-to-channel crosstalk in the optics.
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1. Introduction

The challenge for optoelectronic transceiver design at 10Gbs and above arises from a combination of VCSEL electrical characteristics, high optical channel density, and low optical power/ high gain receiver requirements. 10G VCSELs require high bias currents and large modulation swings. Standard density for such VCSEL arrays is 16 channels/mm^2 or greater. 10G photo receivers must have sensitivity to as little as –20dBm. In this paper we present a unique approach to high speed transceiver design. We focus specifically on 2D channel arrays [1,2,3,4] however the technique is adaptable to linear arrays as well. The key to our new transceiver design is a tight coupling between the digital logic for channel coding and ECC to the layout of the analog cells in the driver array and to the design of the receiver circuits. In the drivers, we are able to directly manipulate signal paths and overall power consumption within the analog circuitry by dynamically revising the channel codes in real time. In the receivers, the same code selection techniques support a new receiver architecture that has similar noise characteristic to differential channels but with substantially higher efficiency in terms of channel utilization.

On the transmitter side a dynamic channel-coding algorithm is used to continuously update the codes used for data transmitted through a particular region of the array. The algorithm is designed to maintain a balance of two parameters, first the overall count and distribution of one-bits in each region of the array and second the variation in total number of one-bits between sequential code words. By manipulating the distribution of 1-bits in a specfic region of the driver array layout, we can control the overall power consumption, increase noise margins, and control crosstalk introduced through the optics and in the receiver arrays. By regulating the changes in the population of one bits between sequential codes, we can maintain consistent supply currents within a region of the driver array thus reducing crosstalk and supply noise within the driver. This technique provides higher (e.g., n of k) coding densities and more robust performance than either “dummy loads” or differential signaling and utilizes the same current-steering drivers.

The channel coding algorithm we use is an adaptation of a channel recoding system that was developed at the University of Pittsburgh under sponsorship by the Air Force Research Laboratory to manage inter-symbol interference within 2D data pages in page oriented optical memory [5]. The original version was designed maximize the noise margin for 2D data pages in the presence of crosstalk between adjacent bits at the detector in the read/write head. This problem is exactly analogous to the transport and detection of 2D arrays of optical communication channels. In simulation studies in our memory research we tested a very dense system with a large crosstalk-induced BER of 10^{-2}. We were able to eliminate all crosstalk induced bit errors in recoded data. The channel coding algorithm had a code rate (code bits/raw data bits) of 77% and ran with constant computation complexity for encoding and decoding.

When adapted to communications channels, we anticipate that this lower crosstalk environment will support even greater efficiency and computational performance. On top of the channel coding, the smart transceivers will implement a distributed ECC for even greater BER reduction. The code is distributed in that ECC encoded data words are reordered in the channel array such that a fixed number of bits from each ECC word appear in each channel-code block. Using an ECC code designed to correct that number of bits, the system will be able to recover full block errors in the channel recoding scheme.

2. Transceiver architecture

Most high speed drivers operate by current "steering". In other words, rather than try to turn on and off VCSEL modulation current at high speed, the modulation current is re-directed either to another VCSEL in a differential pair or to a dummy load for a single ended channel. In either case, these techniques are wasteful of power and/or channel resources. In our new driver design we retain the current steering paradigm, but utilize the array to give the driver circuit more alternatives for the paths along which to steer the modulation current as bits move through the transceiver. Consider the example shown in Figure 1. In this example a 2D array is partitioned into channel code blocks. The new driver design paradigm steers modulation current among the multiple VCSELs within this block.

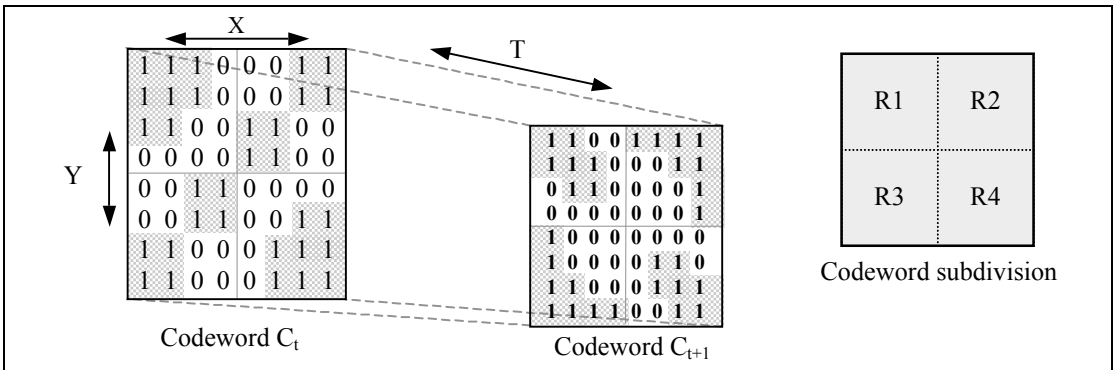

Figure 1: Example of code block partitioning for dynamic channel coding. The 2D channel array is subdivided into four code blocks in this example. Dynamic channel coding balances the distribution of 1-bits with a particular code block and the overall number of 1-bits in successive blocks**.**

This system can only work successfully in concert with a channel coding algorithm that manages the distribution of 0-bits and 1-bits within each code block and keeps the ratio of 0-bits to 1-bits (the bit ratio) between successive code blocks nearly constant. Fortunately, both of these requirements are completely consistent with low noise and low channel-to-channel cross talk for the array.

The overall efficiency of such an approach both in channel utilization and energy consumption is directly related to the code rate of the channel coding system used. Differential coding for example has a code rate of 50%, using 2-bits to send one raw data bit. The simple dynamic channel coding algorithm described below can achieve a 66% code rate for 9-bit blocks.

3. Dynamic channel coding algorithm

The algorithm described below is capable of dynamically changing the way in which data is mapped to code words in the VCSEL driver array. The algorithm can operate in real time, and make changes if necessary on every clock cycle. Code mapping decisions are based only on the incoming raw data, and the last set of code blocks transmitted. The algorithm has constant time complexity and can be easily implemented in 10Gbps logic pipeline logic. Since the algorithm is completely deterministic, the encoding operations are completely reversible by decoder logic based only on the incoming data.

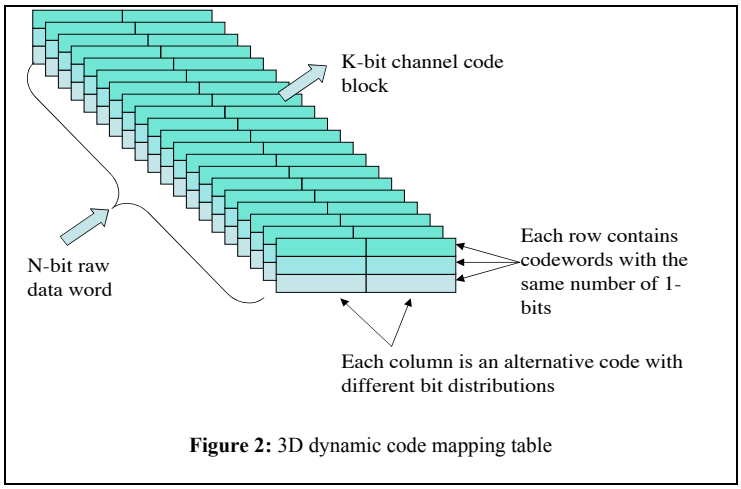

Figure 2: 3D dynamic code mapping table

The algorithm is based on a 3D encoding table organized as shown in Figure 2. The first dimension, shown in the horizontal rows in the figure, organizes the code words by the number of 1-bits in the output mapping. One of the goals is to select mappings that keep the count of 1-bits slowly changing and within a small range. Thus, if the current code is selected from a particular plane in this dimension, we can specify that the next code can only be mapped through the current plane or an immediate neighbor (i.e., to restrict changes to one more or one less 1-bit).

The second dimension is indexed by the raw data word. This is the z-axis dimension in the figure. Each channel code block encodes a fixed number of raw data bits, for example a 9-bit channel code block might typically encode 7-bits of raw data. Thus there would be 64 planes in this dimension. Continuing with the 7/9 code example, if only channel code words with either four or five 1-bits are allowed, there are 252 possible channel codes on which to map the 128 raw data codes. This is the basis for the data in the third dimension of encoding table. This dimension contains a set of alternative code words that can be used for a particular raw data word. There are two alternatives in the 7/9 example. Each alternative has a different topological distribution of 0 and 1 bits and is chosen based on state information for neighboring code blocks. Not all codes have two alternatives, and there are rare cases in which neither of the alternatives for a particular code will work. In this case a reserved, null code is substituted and the data is reordered into the next cycle.

4. Differential receiver array

Figure 3 illustrates the basic concept for our receiver design. Each of the triangles in the figure represents a high speed difference amplifier that compares adjacent bits in a code word group. Thus figure 3a shows a conventional receiver architecture for differential coding and figure 3b and 3c show our extension. By interpreting the differences between adjacent bits rather than magnitude, we achieve the same common mode noise rejection benefits of differential coding. The cost is that this receiver can unambiguously decode only a subset of the allowable n-bit code words for the group. However, this is the same subset already chosen by the dynamic coding algorithm to stabilize the current in the driver circuits.

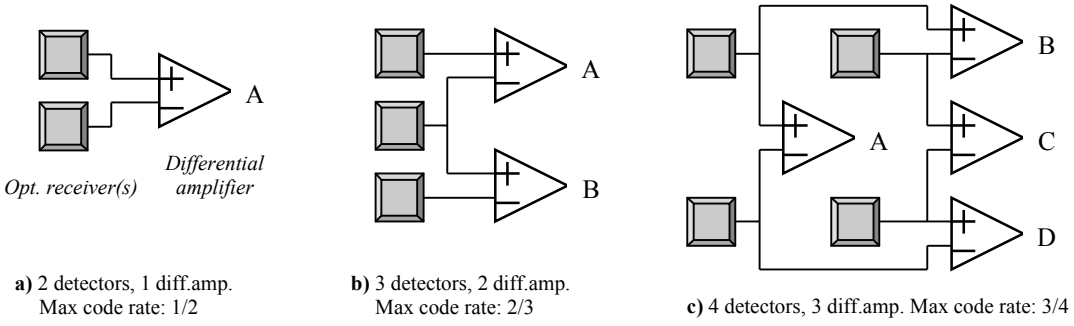

Figure 3: Differential receiver topologies and their potential decoding code rates

Summary

A novel smart transceiver architecture for arrays for optical communication channels has been presented. It is based on balancing the load and current in the VCSEL driver across clusters of bits by dynamically selecting channel code words that support this balance. This code also enables a unique receiver architecture based on high speed difference amplifiers. The result is a transceiver with noise immunity characteristics similar to differentially coded data but with significantly greater channel utilization efficiency.

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