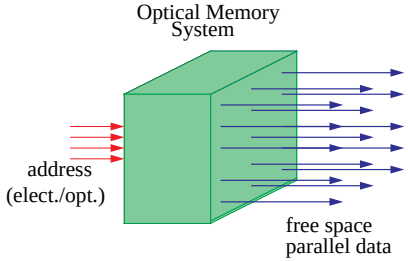
Optoelectronic Cache Memory System Architectures

Donald M. Chiarulli
Department of Computer Science
&
Steven P. Levitan
Department of Electrical Engineering

OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Motivation

Optical memory as an alternative to disks and disk arrays as a backing store for a hierarchical memory system in a general purpose computer

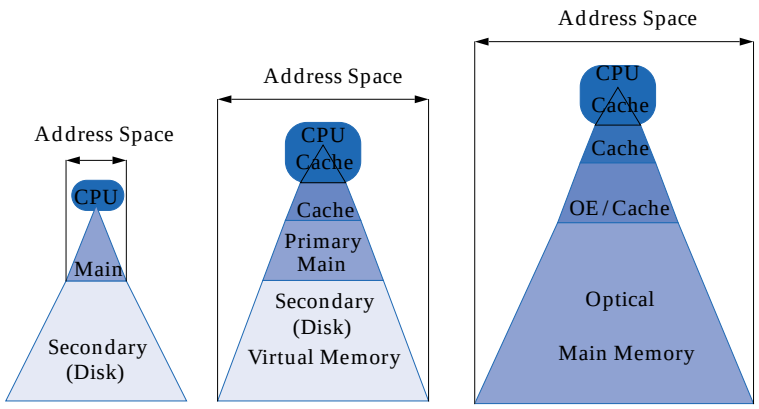


Generic Specifications (near term optical memory device):

- Multi-Terabit Capacity
- 1Mbit free space optical I/O
- 1μs Access Latency

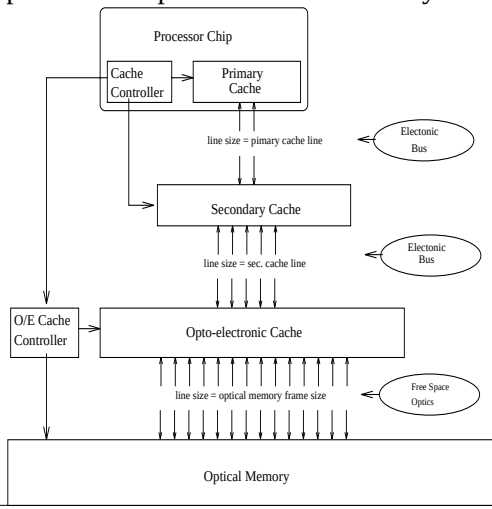
OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Memory Hierarchy Evolution



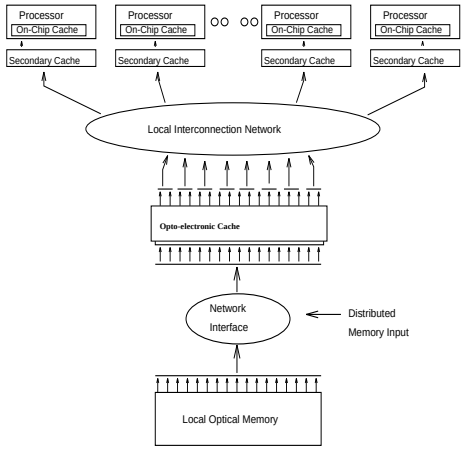
OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Uniprocessor Optoelectronic Memory Hierarchy



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

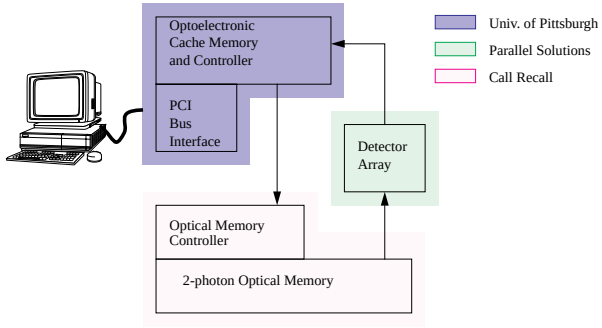
Multiprocessor Optoelectronic Memory Hierarchy



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

UNIVERSITY OF PITTSBURGH

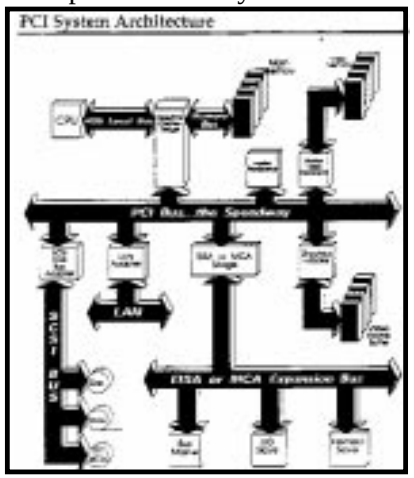
Block Diagram Organized by Participating Research Groups



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

UNIVERSITY OF PITTSBURGH

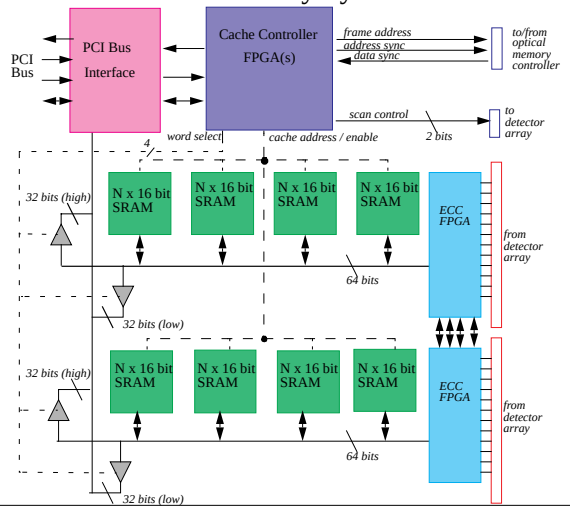
Computer Memory Architecture



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

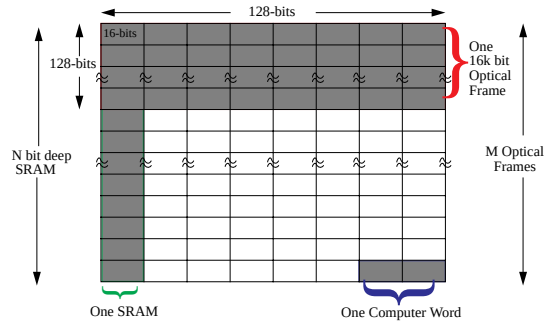
UNIVERSITY OF PITTSBURGH

Cache Memory System



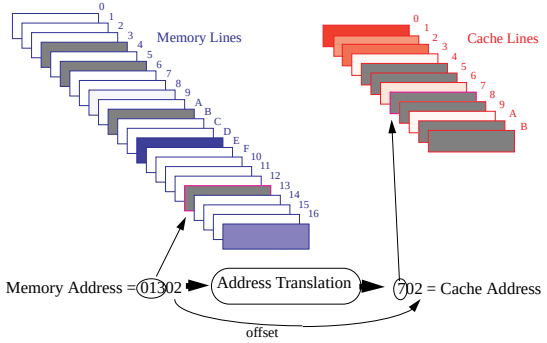
OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Logical Relationship of Optical Memory to Cache Organization



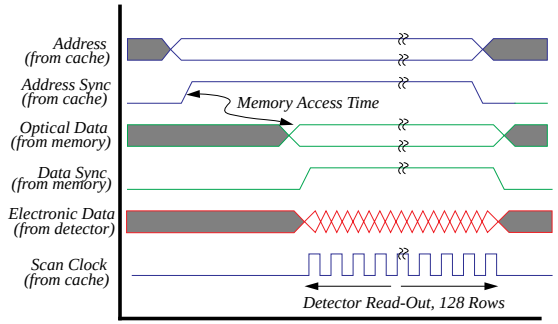
OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Address Translation Between Memory Line 13 and Cache Line 07, offset of 02 is preserved across the translation



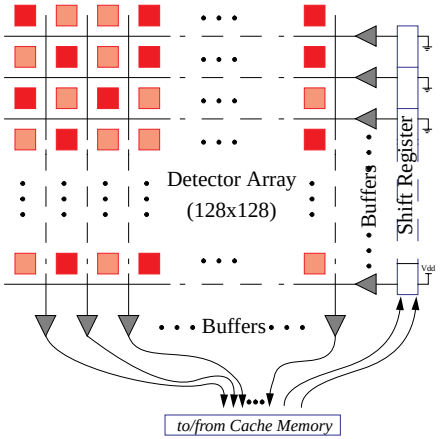
OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

System Timing

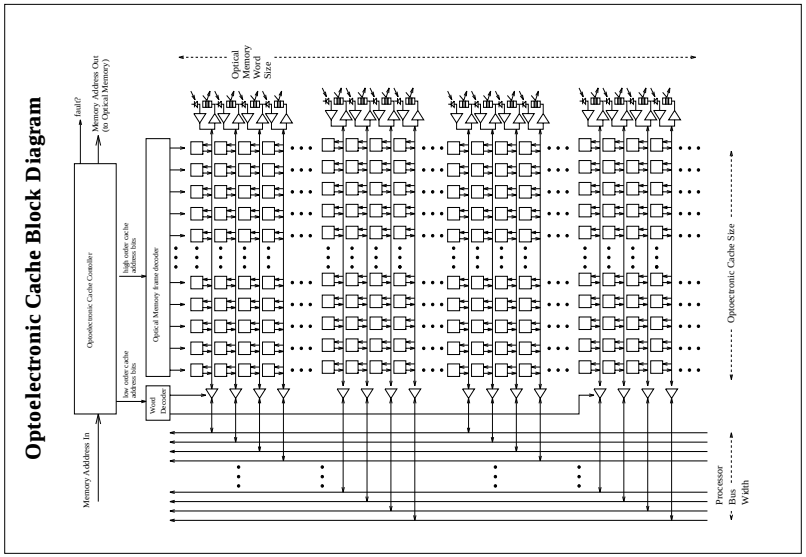


OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Detector Array Organization



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Performance

Run time of a program (ignoring I/O stalls):

- *Run time = instruction count * **CPI** * Clock Rate*

CPI: Clocks Per Instruction

- *CPI = CPU clock cycles*
  *+ (Avg_memoryaccesses * **Avg. memory latency**)*

Average memory Latency at *i-th* level of memory hierarchy

$Avg.\ Memory\ Latency_i = (hit\ latency_i * hit\ rate_i)$
$+ [\mathbf{miss\ penalty}_i * (1\text{-}hit\ rate_i)]$

Miss penalty:

$miss\ penalty_i = Average\ Latency_{i-1}$
$miss\ penalty_0 = Latency_{backing\ store}$

OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Simulation Studies

Three applications

- Image Convolution
- Matrix Multiply
- Heap Sort
-

Three level memory hierarchy - Two Models

- Model 1: Electronic Main Memory / Disk Backing Store
- Model 2: Optoelectronic Cache / Optical Backing Store.
- Primary and Secondary Cache Identical in both models

OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Electronic Memory Simulation Parameters

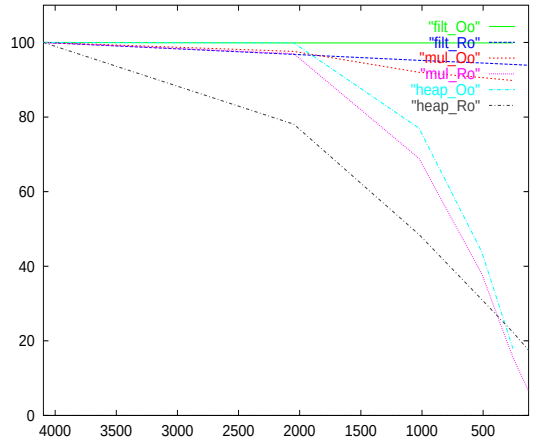
Cache Level	Size	Lines	Line Size	Hit Latency	Miss Penalty
primary	256 Kb	4096	64 bytes	10 ns	(secondary access)
secondary	1 Mb	4096	256 bytes	50 ns	(main memory access)
main memory	64 Mb-to 128 Kb	32K-to-64	2048 bytes	100ns	(disk access)
disk				Seek +Transfer (avg=1ms)	

Optoelectronic Memory Simulation Parameters

Cache Level	Size	Lines	Line Size	Hit Latency	Miss Penalty
primary	128 Kb	4096	16 bytes	10 ns	(secondary access)
secondary	1 Mb	4096	64 bytes	50 ns	(main memory access)
opto-cache	64Mb-to 256Kb	512-to-2	128Kb	100ns	(optical memory access)
optical memory				1000 ns	

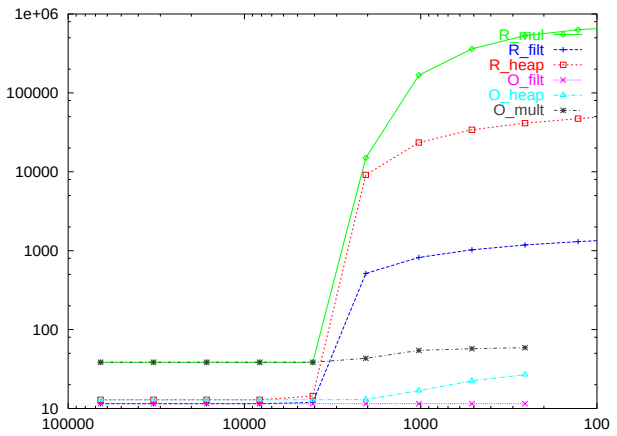
OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Hit Rate (%) vs. Memory Size (Kb)



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Latency (ns) vs. Memory Size (k)



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Research Issues

- What are the appropriate technologies for both the optical memories and the smart pixels used in the cache?
- What are appropriate line sizes, based on current, or near term, fabrication technology?
- What level of internal fragmentation can be tolerated given the lowered fault costs and the limitations on electronic density?
- Given the potential for lowered fault cost, what existing or new address translation mechanisms are best used in this context?
- Given a large line size for the optoelectronic cache, how does this effect the replacement algorithm? Is is possible to devise a new algorithm in which cache lines are overlapped or partially replaced?
- In a multiprocessor application, how should the memory be organized for parallel electronic access relative to the optical memory word size?
- How do the characteristics of the optical memory effect coherency algorithms?
- How do the characteristics of the optical memory effect write policy?

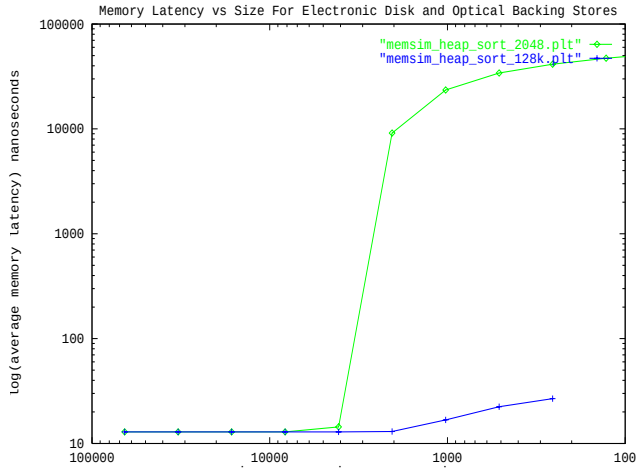
OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

Conclusions

- Smart Pixel Arrays configured as optoelectronic cache memories can be used to effectively interface a low latency optical backing store for an optoelectronic memory hierarchy.
- Although line sizes in the cache are typically larger than disk-pages, average memory latency is not adversely affected by the additional internal fragmentation introduced.
- Performance gains of 3 to 4 orders of magnitude are possible with near term technology.

OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

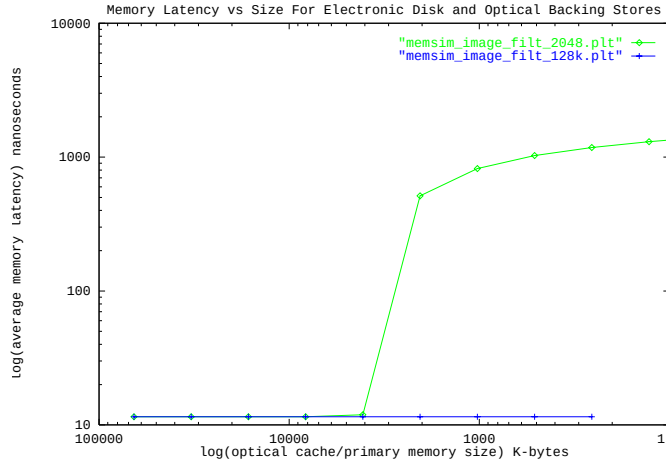
Heap Sort



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

UNIVERSITY OF PITTSBURGH

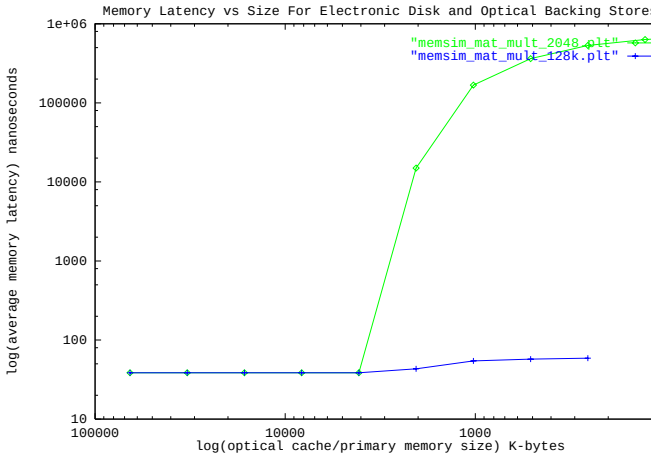
Image Filter



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

UNIVERSITY OF PITTSBURGH

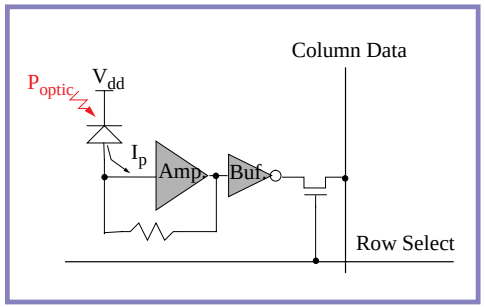
Matrix Multiply



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

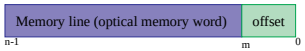
UNIVERSITY OF PITTSBURGH

Typical Detector Circuit



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663

OE Cache Address Consisting of Optical Memory Word and Offset



OPTOELECTRONIC COMPUTING SYSTEMS
DEPARTMENTS OF COMPUTER SCIENCE & ELECTRICAL ENGINEERING
UNIVERSITY OF PITTSBURGH
PITTSBURGH, PA 15260
+1-412-624-8839 +1-412-648-9663