An Optically Reconfigurable Field Programmable Gate Array*

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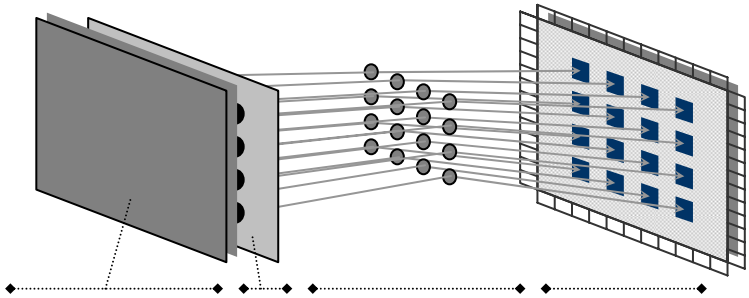
Introduction

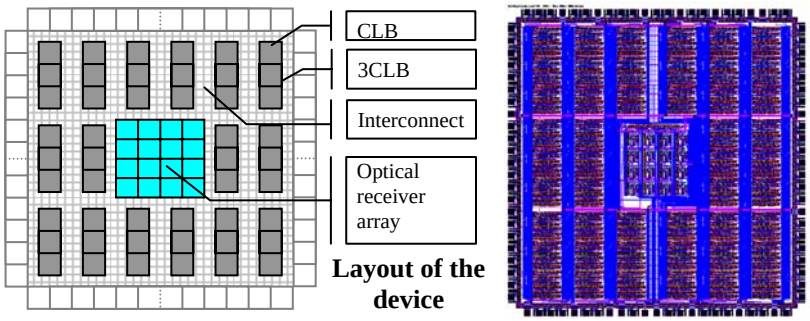
We have developed an optically reconfigurable field programmable gate array (OFPGA). The OFPGA integrated circuit is designed for high-speed configuration in systems based on a reconfigurable computing paradigm [1]. In these environments, the computation resources provided by the FPGA re-used in multiple configurations throughout a single application program. Example applications are image and signal processing, data compression and database operations. In these applications, the same FPGA could be used to perform floating-point operations, histogramming, and query processing [2].



Optically Reconfigurable System

Chip Architecture

The OFPGA consists of 48 3-input configurable logic blocks (CLB), which can send and receive signals via configurable interconnect. The configuration data can be uploaded optically using 4x4 optical receiver array. The same array can be used as optical data input, when the device executes the configuration.



Layout of the device

The CLBs are arranged in a 6 x 9 grid. In the middle of the grid in the place of 2x3 CLBs reside the optical receiver array. All CLBs are divided in groups of three (3CLB). There are 16 3CLB groups. Each of those groups receives separate optical signal for configuration by the optical receiver array, if configured optically. Therefore, all of the 3CLB groups can be configured simultaneously, even though the configurations are different. Each of the CLB in a 3CLB group can be configured separately. This makes partial device configuration possible.

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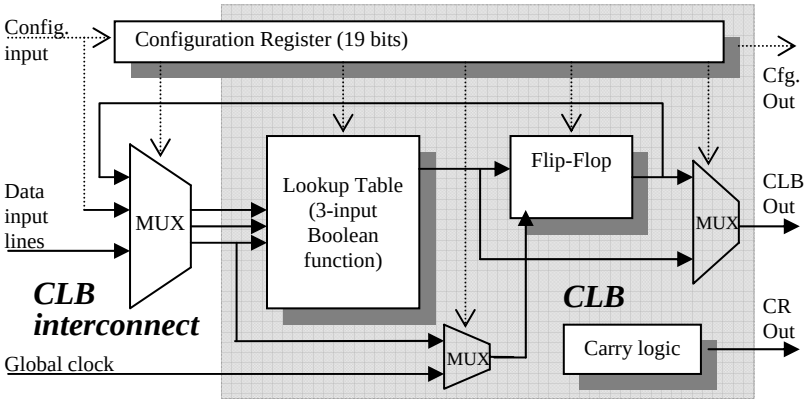
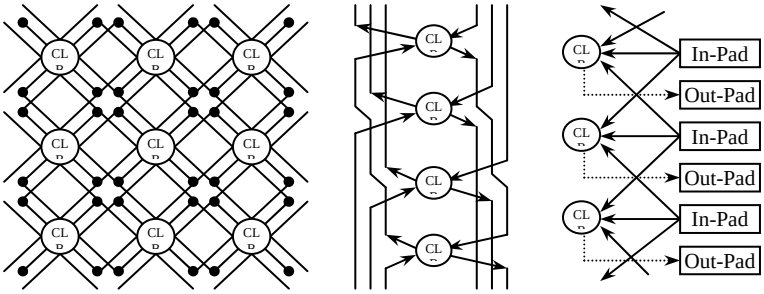
Configurable Logic Block Design

The configurable logic blocks (CLBs) [3] are composed of a bit serial configuration register, input ultiplexer, a programmable Boolean logic function, and a flip-flop. Since configuration input data line may carry information from the optical receivers, we can use it as an "optical" input for the CLB. The flip-flop can be clocked by either a global clock signal or one of the inputs of the CLB. Thus, the flip-flop can be used for either data storage or frequency divider. Finally, the CLB has carry logic and a carry output signal, that allows it to be used as a full adder and combined with other CLBs to make an n-bit adder.



Interconnect

The interconnect provides routing of the following classes of signals: *Short* – CLB to any of its 8 immediate neighbor CLBs; *Long* – CLB to some of the other CLBs that are 3 interconnect units distant; *I/O* – perimeter CLB inputs and outputs to the I/O pins of the device; *Global In* – global data from input pins to all CLBs; *Carry* – carry signal routing when the CLBs are used as Full Adders. *Optic* – signals received by optical receiver array to the inputs of the CLBs; *Control* lines, such as clock, configuration data and enable signals.



"Short" interconnect *"Long" interconnect* *"I/O" interconnect*

Optical Receiver Array

The optical information can be received by 4x4 array of receiver cells [4]. Each cell has two optical detectors (17μm and 34μm) that differ in sensitivity and speed. The receiver array is located in the middle of the chip. The receiver cell pitch is 250 microns, the same as the pitch of typical VCSEL arrays that would be used as transmitters of the optical configuration data.

Configuration Modes

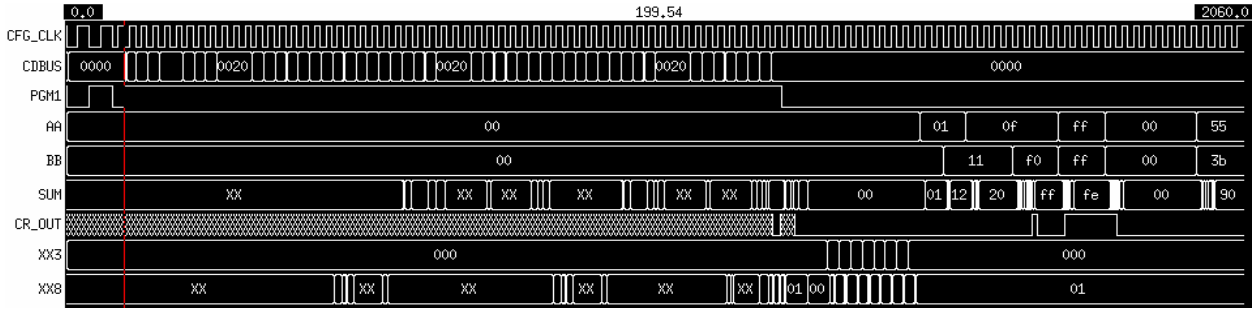
The configuration data for one CLB and its related interconnect fits in 19 bits of information. This information is clocked in serially for each CLB. There are 4 possible configuration modes: 2 optical and 2 electrical. The optical ones differ by the size of optical detectors they use. The electrical configuration modes provide fast "all-same" or "all-different" configuration options. For both optical modes the 3CLB groups are configured in parallel, thus only 19x3 = 56 clock cycles are necessary to configure the whole device. In the third mode, the configuration data is input serially, thus requiring 19x48 = 912 clock cycles for the whole device. For the fourth mode, used for testing, all the CLBs receive the same configuration data; thus, the system can be configured in only 19 clock cycles.

Performance

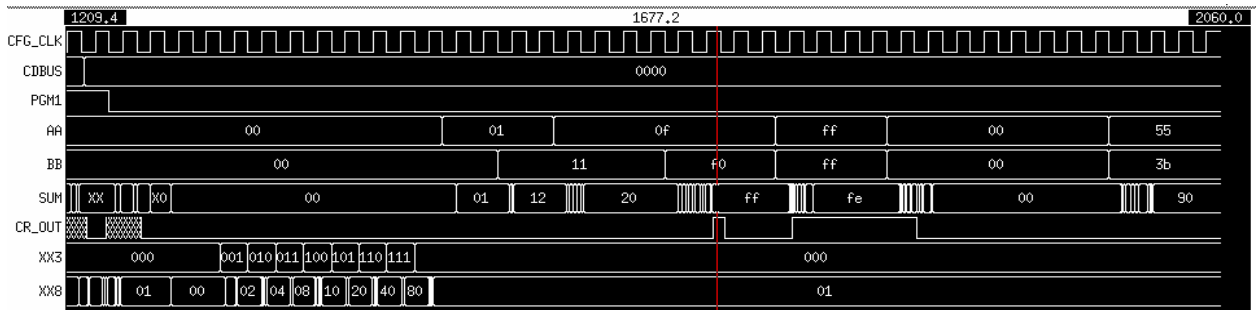
The simulation results reveal that the maximum clock frequency for the chip will be at least 50MHz. Therefore, in the worst case, the full configuration of the device in each of the configuration modes is:

Modes	*Time (ns)*	*Clock cycles*	*Comments*
1 and 2 (optical)	1140 ns	3 x 19 = 57	3 sets of CLBs require 3 x 19 clock cycles
3 (electrical)	18240 ns	48 x 19 = 912	All the configuration is uploaded serially
4 (electrical)	380 ns	19	All CLBs receive the same configuration

In the illustration below, we can see a test case where the configuration is loaded using mode 1. The load phase is indicated by active-high signal PGM1. The CDBUS signal illustrates the configuration data being transferred. The waveform diagram shows the load taking 1140ns at 50Mhz.



Next, we show a close-up where the configuration is complete, and the adder and decoder are tested:



The configuration in this case defines one full 8-bit ripple carry adder and an independent 3-to-8 decoder. The signals AA and BB are the inputs for the adder while the SUM and CR_OUT are outputs. Similarly, the signals XX3 and XX8 are inputs and outputs of the 3-to-8 decoder. The worst case delay for the decoder is 12ns from input change to output change. For the ripple carry adder, the delay is higher – about 33ns in the worst case.

Discussion

The OFPGA has been designed as a proof-of-concept prototype with fabrication in 1.2 um SCMOS technology. State of the art systems use smaller feature sizes that allow faster operation speeds, more optical detectors and increased CLB count. Thus, one can foresee OFPGA circuits with hundreds of CLBs and configuration times under a microsecond. This would enable a new class of high-speed reconfigurable processors based on optoelectronic technology.

References

[1] M.F. Sakr, et al., Optics in Computing '98, Proceedings of SPIE Vol. 3490, pp. 564-7 (1998).
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[4] D.A. Van Blerkom, et al., Journal of Lightwave Technology, vol.16, no.1, IEEE, p.119-26, January 1998.