3D-OptoElectronic Stacked Processors: Technology Development

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All-electronic systems remain inadequate when the manipulation and processing of large data sets is required, for example, in image processing and understanding applications. Although many parallel algorithms exist in this domain, their mapping on existing system architectures usually leads to unsatisfactory performance when the data sets are large. New hardware solutions capable of switching and routing data at very high speeds for performing operations such as histogram, centroid, moment, segmentation and FFT calculations are critically needed for the implementation of real time and adaptive signal processing systems. Important applications can be addressed, if such operations could be performed on 1024x1024 data arrays with 32 bit accuracy at fast-frame video rates, with power and volume efficient hardware components, making such systems easily portable.

One way of approaching single chip like performance using a multi-chip set can be achieved by 3-D packaging at the chip level, for example by stacking chips together. Each chip in the stack communicates with its neighbors using electrical interconnects deposited on the sides of the stack. This approach reduces the length of the chip to chip interconnects by placing the neighboring chips in very close proximity of each other. However, this approach can not support the density and globality of interconnects that are required by many operations when a stack contains many chips or when the overall system consists of several stacks. Furthermore, by modeling and projecting the future performance of electrical and optoelectronic interconnections, it can be shown that free-space optoelectronic links have a power-delay advantage of 10 to 50 over their electrical counterparts at room temperature for systems handling large data sets. In this case, free-space optics provides the much needed low power, global, high density interconnects to communicate between chips in large stacks or between stacks.

By utilizing the combined strengths of 3-D chip packaging and optoelectronic array interconnect technologies, it is possible to bring a low-power ultra-compact hardware solution to systems requiring fast processing and handling of large data arrays. We believe that, providing optoelectronic I/O to 3-D chip stacks using VCSEL arrays with associated drivers, specially designed optical receivers, and micro-optics to direct the optical signals provide the most efficient way to communicate between the stacks. By integrating these components with a set of packaging techniques ranging from silicon micro-bench to plastic molded lenses, we are presently engaged in demonstrating the practical superiority of this approach in terms of system speed, power and volume metrics. This talk will address various aspects of this approach that is being explored within the 3-D OESP consortium.

The "3D OptoElectronic Stacked Processors" industry-university consortium [1] has been created to explore the use of optical interconnections within computers. This effort is cost shared by the Defense Advanced Research Projects Agency (DARPA), Rome Laboratory, and 12 participating companies and universities. The participating Universities are the University of California at San Diego, the Georgia Institute of Technology, the University of Pittsburgh, the University of North Carolina at Charlotte, the University of California at Los Angeles, and the University of California at Santa Barbara. The industrial participants include the Honeywell Technology Center, Irvine Sensors Corporation, Kopin Corporation, Mercury Computer Systems, Sun Microsystems, and Duet Technologies. Among the consortium members, UCSD provides expertise in system architecture, optical system design, VLSI design, system integration and testing, and thermal modeling. Honeywell is a leader in vertical cavity laser and photodetector development while UC Santa Barbara provides theoretical and next generation device expertise in these technologies. Kopin Corporation and Georgia Institute Technology are involved

in experimental micro laser integration based on epitaxial lift-off. lrvine Sensors contributes technology for three-dimensional stacking of VLSI circuits, a strategy that saves volume while potentially increasing the performance of multi-chip systems and will also act as the final system integrator in the prototypes that the consortium will assemble. The University of Pittsburgh directs the system modeling and simulations while the University of North Carolina Charlotte, with the assistance of Duet, concentrates on the design and testing of the electronic chips. Sun Microsystems and Mercury Computer Systems assist in the overall project direction and identify potential commercial and government applications. Finally, the team from UCLA leads the efforts to insert new silicon based technologies (silicon microbench, MEMs) to tackle the system packaging issues.

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1 Fotr more information, see http://soliton.ucsd.edu/3doesp